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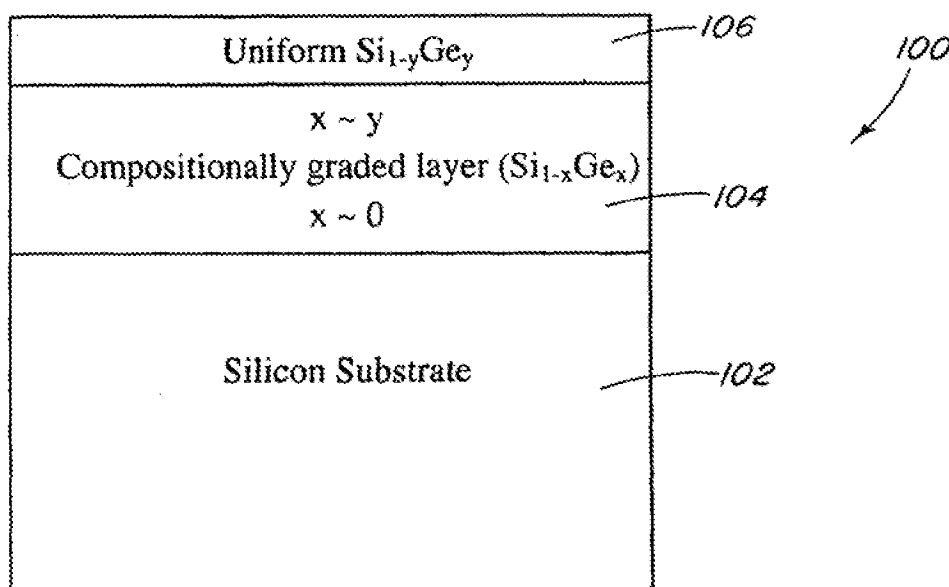
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(54) Title: RELAXED SILICON GERMANIUM PLATFORM FOR HIGH SPEED CMOS ELECTRONICS AND HIGH SPEED ANALOG CIRCUITS



(57) Abstract: Structures and methods for fabricating high speed digital, analog, and combined digital/analog systems using planarized relaxed SiGe as the materials platform. The relaxed SiGe allows for a plethora of strained Si layers that possess enhanced electronic properties. By allowing the MOSFET channel to be either at the surface or buried, one can create high-speed digital and/or analog circuits. The planarization before the device epitaxial layers are deposited ensures a flat surface for state-of-the-art lithography.

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**RELAXED SILICON GERMANIUM PLATFORM FOR
HIGH SPEED CMOS ELECTRONICS AND HIGH SPEED ANALOG
CIRCUITS**

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PRIORITY INFORMATION

This application claims priority from U.S. Patent Applications Nos. 09/906,200 and 09/906,201 both filed on July 16, 2001, which claim priority to U.S. provisional application Ser. No. 60/273,112 filed March 2, 2001.

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BACKGROUND OF THE INVENTION

The invention relates to the field of relaxed SiGe platforms for high speed CMOS electronics and high speed analog circuits.

Si CMOS as a platform for digital integrated circuits has progressed predictably through the industry roadmap. The progress is created through device miniaturization, leading to higher performance, greater reliability, and lower cost. However, new bottlenecks in data flow are appearing as the interconnection hierarchy is expanded. Although digital integrated circuits have progressed at unprecedented rates, analog circuitry has hardly progressed at all. Furthermore, it appears that in the near future, serious economic and technological issues will confront the progress of digital integrated circuits.

The digital and communication chip markets need an enhancement to Si CMOS and the maturing roadmap. One promising candidate material that improves digital integrated circuit technology and introduces new analog integrated circuit possibilities is relaxed SiGe material on Si substrates. Relaxed SiGe alloys on Si can have thin layers of Si deposited on them, creating tension in the thin Si layers. Tensile Si layers have many advantageous properties for the basic device in integrated circuits, the metal-oxide field effect transistor (MOSFET). First, placing Si in tension increases the mobility of electrons moving parallel to the surface of the wafer, thus increasing the frequency of operation of the MOSFET and the associated circuit. Second, the band offset between the relaxed SiGe and the tensile Si will confine electrons in the Si layer. Therefore, in an electron channel device (n-channel), the channel can be removed from the surface or 'buried'. This ability to spatially separate the charge carriers from scattering centers such as ionized impurities and the 'rough' oxide interface enables the production of low noise, high performance analog devices and circuits.

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A key development in this field was the invention of relaxed SiGe buffers with low

threading dislocation densities. The key background inventions in this area are described in U.S. Pat. No. 5,442,205 issued to Brasen et al. and U.S. Pat. No. 6,107,653 issued to Fitzgerald. These patents define the current best methods of fabricating high quality relaxed SiGe.

5 Novel device structures in research laboratories have been fabricated on early, primitive versions of the relaxed buffer. For example, strained Si, surface channel nMOSFETs have been created that show enhancements of over 60% in intrinsic μ_n with electron mobility increases of over 75% (Rim et al, IEDM 98 Tech. Dig. p. 707). Strained Si, buried channel devices demonstrating high transconductance and high
10 mobility have also been fabricated (U. Konig, MRS Symposium Proceedings 533, 3 (1998)). Unfortunately, these devices possess a variety of problems with respect to commercialization. First, the material quality that is generally available is insufficient for practical utilization, since the surface of SiGe on Si becomes very rough as the material is relaxed via dislocation introduction. These dislocations are essential in the
15 growth of relaxed SiGe layers on Si since they compensate for the stress induced by the lattice mismatch between the materials. For more than 10 years, researchers have tried to intrinsically control the surface morphology through epitaxial growth, but since the stress fields from the misfit dislocations affect the growth front, no intrinsic epitaxial solution is possible. The invention describes a method of planarization and regrowth
20 that allows all devices on relaxed SiGe to possess a significantly flatter surface. This reduction in surface roughness increases the yield for fine-line lithography, thus enabling the manufacture of strained Si devices.

A second problem with the strained Si devices made to date is that researchers have been concentrating on devices optimized for very different applications. The
25 surface channel devices have been explored to enhance conventional MOSFET devices, whereas the buried channel devices have been constructed in ways that mimic the buried channel devices previously available only in III-V materials systems, like AlGaAs/GaAs. Recognizing that the Si manufacturing infrastructure needs a materials platform that is compatible with Si, scalable, and capable of being used in the plethora
30 of Si integrated circuit applications, the disclosed invention provides a platform that allows both the enhancement of circuits based on Si CMOS, as well as the fabrication of analog circuits. Thus, high performance analog or digital systems can be designed with this platform. An additional advantage is that both types of circuits can be fabricated in the CMOS process, and therefore a combined, integrated digital/analog
35 system can be designed as a single-chip solution.

With these advanced SiGe material platforms, it is now possible to provide a variety of device and circuit topologies that take advantage of this new materials system. Exemplary embodiments of the invention describe structures and methods to fabricate advanced strained-layer Si devices, and structures and methods to create circuits based on a multiplicity of devices, all fabricated from the same starting material platform. Starting from the same material platform is key to minimizing cost as well as to allowing as many circuit topologies to be built on this platform as possible.

SUMMARY OF THE INVENTION

Accordingly, the invention provides a material platform of planarized relaxed SiGe with regrown device layers. The planarization and regrowth strategy allows device layers to have minimal surface roughness as compared to strategies in which device layers are grown without planarization. This planarized and regrown platform is a host for strained Si devices that can possess optimal characteristics for both digital and analog circuits. Structures and processes are described that allow for the fabrication of high performance digital logic or analog circuits, but the same structure can be used to host a combination of digital and analog circuits, forming a single system-on-chip.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic block diagram of a structure including a relaxed SiGe layer epitaxially grown on a Si substrate;

FIG. 2 is a schematic block diagram of an exemplary structure showing that the origin of the crosshatch pattern is the stress fields from injected misfit dislocations;

FIG. 3 is a table showing surface roughness data for relaxed SiGe buffers produced by dislocation injection via graded SiGe layers on Si substrates;

FIGs. 4A-4D show an exemplary process flow and resulting platform structure in accordance with the invention;

FIGs. 5A-5D are schematic diagrams of the corresponding process flow and layer structure for a surface channel FET platform in accordance with the invention;

FIGs. 6A-6D are schematic diagrams of the corresponding process flow and layer structure for a buried channel FET platform in accordance with the invention;

FIGs. 7A-7D are schematic diagrams of a process flow for a surface channel MOSFET in accordance with the invention;

FIGs. 8A and 8B are schematic block diagrams of surface channel devices with

protective layers;

FIGs. 9A and 9B are schematic block diagrams of surface channel devices with Si layers on Ge-rich layers for use in silicide formation;

FIGs. 10 is schematic diagram of a buried channel MOSFET after device
5 isolation in accordance with the invention;

FIG. 11 is a schematic flow of the process, for any heterostructure FET device deposited on relaxed SiGe, in accordance with the invention;

FIGs. 12A-12D are schematic diagrams of a process flow in the case of forming the surface channel MOSFET in the top strained Si layer in accordance with the
10 invention;

FIGs. 13A-13D are schematic diagrams of a process flow in the case of forming the surface channel MOSFET in the buried strained Si layer in accordance with the invention; and

FIGs. 14A and 14B are schematic diagrams of surface and buried channel
15 devices with $\text{Si}_{1-y}\text{Ge}_y$ channels on a relaxed $\text{Si}_{1-x}\text{Ge}_x$ layer.

DETAILED DESCRIPTION OF THE INVENTION

FIG. 1 is a schematic block diagram of a structure 100 including a relaxed SiGe layer epitaxially grown on a Si substrate 102. In this structure, a compositionally
20 graded buffer layer 104 is used to accommodate the lattice mismatch between the uniform SiGe layer 106 and the Si substrate. By spreading the lattice mismatch over a distance, the graded buffer minimizes the number of dislocations reaching the surface and thus provides a method for growing high-quality relaxed SiGe films on Si.

Any method of growing a high-quality, relaxed SiGe layer on Si will produce
25 roughness on the surface of the SiGe layer in a well-known crosshatch pattern. This crosshatch pattern is typically a few hundred angstroms thickness over distances of microns. Thus, the crosshatch pattern is a mild, undulating surface morphology with respect to the size of the electron or hole. For that reason, it is possible to create individual devices that achieve enhancements over their control Si device counterparts.
30 However, commercialization of these devices requires injection of the material into the Si CMOS process environment to achieve low cost, high performance targets. This processing environment requires that the material and device characteristics have minimal impact on the manufacturing process. The crosshatch pattern on the surface of the wafer is one limiting characteristic of relaxed SiGe on Si that affects the yield and
35 the ease of manufacture. Greater planarity is desired for high yield and ease in

lithography.

The origin of the crosshatch pattern is the stress fields from the injected misfit dislocations. This effect is depicted by the exemplary structure 200 shown in FIG. 2. By definition, the dislocations must be introduced in order to accommodate the lattice-mismatch between the SiGe alloy and the Si substrate. The stress fields originate at the dislocations, and are terminated at the surface of the film. However, the termination at the surface creates crystal lattices that vary from place to place on the surface of the wafer. Since growth rate can be correlated to lattice constant size, different thicknesses of deposition occur at different points on the wafer. One may think that thick layer growth beyond the misfit dislocations will smooth the layer of these thickness differences. Unfortunately, the undulations on the surface have a relatively long wavelength; therefore, surface diffusion is typically not great enough to remove the morphology.

FIG. 3 is a table that displays surface roughness data for relaxed SiGe buffers produced by dislocation injection via graded SiGe layers on Si substrates. Note that the as-grown crosshatch pattern for relaxed $\text{Si}_{0.8}\text{Ge}_{0.2}$ buffers creates a typical roughness of approximately 7.9nm. This average roughness increases as the Ge content in the relaxed buffer is increased. Thus, for any SiGe layer that is relaxed through dislocation introduction during growth, the surface roughness is unacceptable for state-of-the-art fabrication facilities. After the process in which the relaxed SiGe is planarized, the average roughness is less than 2nm (typically 0.57nm), and after device layer deposition, the average roughness is 0.77nm with a 1.5 μm regrowth thickness. Therefore, after the complete structure is fabricated, over one order of magnitude of roughness reduction can be achieved.

The regrowth device layers can be either greater than or less than the critical thickness of the regrowth layer. In general, in any lattice-mismatched epitaxial growth, thin layers can be deposited without fear of dislocation introduction at the interface. At a great enough thickness, any lattice-mismatch between the film and substrate will introduce misfit dislocations into the regrown heterostructure. These new dislocations can cause additional surface roughness. Thus, if the lattice-mismatch between the regrowth device layers and relaxed SiGe buffer is too great, the effort of planarizing the relaxed SiGe may be lost since massive dislocation introduction will roughen the surface.

There are two distinct possibilities with respect to the regrowth thickness and the quality of surface. If the regrowth layers are very thin, then exact lattice matching of the

regrowth layer composition and the relaxed buffer composition is not necessary. In this case, the surface roughness will be very low, approximately equal to the post-planarization flatness. However, in many applications for devices, the regrowth layer thickness will be 1-2 μ m or more. For a 1% difference in Ge concentration between the relaxed SiGe and the regrowth layer, the critical thickness is approximately 0.5 μ m. Thus, if optimal flatness is desired, it is best to keep the regrowth layer below approximately 0.5 μ m unless excellent control of the uniformity of Ge concentration across the wafer is achieved. Although this composition matching is achievable in state-of-the-art tools, FIG. 3 shows that less precise matching, i.e., within 2% Ge, results in misfit dislocation introduction and introduction of a new crosshatch pattern. However, because the lattice mismatch is so small, the average roughness is still very low, approximately 0.77nm. Thus, either lattice-matching or slight mismatch will result in excellent device layer surfaces for processing.

It is also noted that the relaxed SiGe alloy with surface roughness may not necessarily be a uniform composition relaxed SiGe layer on a graded composition layer. Although this material layer structure has been shown to be an early example of high quality relaxed SiGe, there are some disadvantages to this structure. For example, SiGe alloys possess a much worse coefficient of thermal conductivity than pure Si. Thus, for electronic devices located at the surface, it may be relatively difficult to guide the heat away from the device areas due to the thick graded composition layer and uniform composition layer.

Another exemplary embodiment of the invention, shown in FIGs. 4A-4D, solves this problem and creates a platform for high power SiGe devices. FIGs. 4A-4D show an exemplary process flow and resulting platform structure in accordance with the invention. The structure is produced by first forming a relaxed uniform SiGe alloy 400 via a compositionally graded layer 402 on a Si substrate 404. The SiGe layer 400 is then transferred to a second Si substrate 406 using conventional bonding. For example, the uniform SiGe alloy 400 on the graded layer 402 can be planarized to remove the crosshatch pattern, and that relaxed SiGe alloy can be bonded to the Si wafer. The graded layer 402 and the original substrate 404 can be removed by a variety of conventional processes. For example, one process is to grind the original Si substrate away and selectively etch to the SiGe, either by a controlled dry or wet etch, or by embedding an etch stop layer. The end result is a relaxed SiGe alloy 400 on Si without the thick graded layer. This structure is more suited for high power applications since the heat can be conducted away from the SiGe layer more efficiently. The bond and substrate removal technique can also be used to produce SiGe on insulator substrates, or SGOI. An SGOI

wafer is produced using the same technique shown in FIGs. 4A-4D; however, the second substrate is coated with a SiO₂ layer before bonding. In an alternative embodiment, both wafers can be coated with SiO₂ to enable oxide-to-oxide bonding. The resulting structure after substrate removal is a high quality, relaxed SiGe layer on an insulating film. Devices
5 built on this platform can utilize the performance enhancements of both strained Si and the SOI architecture.

It will be appreciated that in the scenario where the SiGe layer is transferred to another host substrate, one may still need to planarize before regrowing the device layer structure. The SiGe surface can be too rough for state of the art processing due to the
10 substrate removal technique. In this case, the relaxed SiGe is planarized, and the device layers are regrown on top of the high-quality relaxed SiGe surface.

Planarization of the surface via mechanical or other physical methods is required to flatten the surface and to achieve CMOS-quality devices. However, the field effect transistors (FETs) that allow for enhanced digital and analog circuits are
15 very thin, and thus would be removed by the planarization step. Thus, a first part of the invention is to realize that relaxed SiGe growth and planarization, followed by device layer regrowth, is key to creating a high-performance, high yield enhanced CMOS platform. FIGs. 5 and 6 show the process sequence and regrowth layers required to create embodiments of surface channel and buried channel FETs, respectively.

20 FIGs. 5A-5D are schematic diagrams of a process flow and resulting layer structure in accordance with the invention. FIG. 5A shows the surface roughness 500, which is typical of a relaxed SiGe alloy 502 on a substrate 504, as an exaggerated wavy surface. Note that the substrate is labeled in a generic way, since the substrate could itself be Si, a relaxed compositionally graded SiGe layer on Si, or another material in
25 which the relaxed SiGe has been transferred through a wafer bonding and removal technique. The relaxed SiGe alloy 502 is planarized (FIG. 5B) to remove the substantial roughness, and then device regrowth layers 506 are epitaxially deposited (FIG. 5C). It is desirable to lattice-match the composition of the regrowth layer 506 as closely as possible to the relaxed SiGe 502; however, a small amount of mismatch and
30 dislocation introduction at the interface is tolerable since the surface remains substantially planar. For a surface channel device, a strained Si layer 508 of thickness less than 0.1 μm is then grown on top of the relaxed SiGe 502 with an optional sacrificial layer 510, as shown in FIG. 5D. The strained layer 508 is the layer that will be used as the channel in the final CMOS devices.

35 FIGs. 6A-6D are schematic diagrams of the corresponding process flow and layer structure

for a buried channel FET platform in accordance with the invention. In this structure, the regrowth layers 606 include a lattice matched SiGe layer 602, a strained Si channel layer 608 with a thickness of less than $0.05\mu\text{m}$, a SiGe separation or spacer layer 612, a Si gate oxidation layer 614, and an optional sacrificial layer 610 used to protect the heterostructure during the initial device processing steps.

Once the device structure has been deposited, the rest of the process flow for device fabrication is very similar to that of bulk Si. A simplified version of the process flow for a surface channel MOSFET in accordance with the invention is shown in FIGs. 7A-7D. This surface channel MOSFET contains a relaxed SiGe layer 700 and a strained Si layer 702. The device isolation oxide 704, depicted in FIG. 7A, is typically formed first. In this step, the SiN layer 706, which is on top of a thin pad oxide layer 708, serves as a hard mask for either local oxidation of silicon (LOCOS) or shallow trench isolation (STI). Both techniques use a thick oxide (relative to device dimensions) to provide a high threshold voltage between devices; however, STI is better suited for sub-quarter-micron technologies. Figure 7B is a schematic of the device area after the gate oxide 716 growth and the shallow-source drain implant. The implant regions 710 are self-aligned by using a poly-Si gate 712 patterned with photoresist 714 as a masking layer. Subsequently, deep source-drain implants 718 are positioned using conventional spacer 720 formation and the device is electrically contacted through the formation of silicide 722 at the gate and silicide/germanides 724 at the source and drain (Figure 7C). Figure 7D is a schematic of the device after the first level of metal interconnects 726 have been deposited and etched.

Since there are limited-thickness layers on top of the entire structure, the removal of surface material during processing becomes more critical than with standard Si. For surface channel devices, the structure that is regrown consists primarily of nearly lattice-matched SiGe, and a thin surface layer of strained Si. Many of the processes that are at the beginning of a Si fabrication sequence strip Si from the surface. If the processing is not carefully controlled, the entire strained Si layer can be removed before the gate oxidation. The resulting device will be a relaxed SiGe channel FET and thus the benefits of a strained Si channel will not be realized.

A logical solution to combat Si removal during initial processing is to make the strained Si layer thick enough to compensate for this removal. However, thick Si layers are not possible for two reasons. First, the enhanced electrical properties originate from the fact that the Si is strained and thick layers experience strain relief through the introduction of misfit dislocations. Second, the misfit dislocations themselves are

undesirable in significant quantity, since they can scatter carriers and increase leakage currents in junctions.

In order to prevent removal of strained Si layers at the surface, the cleaning procedures before gate oxidation must be minimized and/or protective layers must be applied. Protective layers are useful since their removal can be carefully controlled. Some examples of protective layers for surface channel devices are shown in FIGS. 8A and 8B. FIG. 8A shows a strained Si heterostructure of a relaxed SiGe layer 800 and a strained Si channel layer 802 protected by a surface layer 804 of SiGe. The surface SiGe layer 804 should have a Ge concentration similar to that of the relaxed SiGe layer 800 below, so that the thickness is not limited by critical thickness constraints. During the initial cleans, the SiGe sacrificial layer is removed instead of the strained Si channel layer. The thickness of the sacrificial layer can either be tuned to equal the removal thickness, or can be made greater than the removal thickness. In the latter case, the excess SiGe can be selectively removed before the gate oxidation step to reveal a clean, strained Si layer at the as grown thickness. If the particular fabrication facility prefers a Si terminated surface, a sacrificial Si layer may be deposited on top of the SiGe sacrificial cap layer.

FIG. 8B shows a structure where a layer 806 of SiO₂ and a surface layer 808 of either a poly-crystalline or an amorphous material are used as protective layers. In this method, an oxide layer is either grown or deposited after the epitaxial growth of the strained Si layer. Subsequently, a polycrystalline or amorphous layer of Si, SiGe, or Ge is deposited. These semiconductor layers protect the strained-Si layer in the same manner as a SiGe cap during the processing steps before gate oxidation. Prior to gate oxidation, the poly/amorphous and oxide layers are selectively removed. Although the sacrificial layers are shown as protection for a surface channel device, the same techniques can be employed in a buried channel heterostructure.

Another way in which conventional Si processing is modified is during the source-drain silicide-germanide formation (FIG. 7C). In conventional Si processing, a metal (typically Ti, Co, or Ni) is reacted with the Si and, through standard annealing sequences, low resistivity silicides are formed. However, in this case, the metal reacts with both Si and Ge simultaneously. Since the silicides have much lower free energy than the germanides, there is a tendency to form a silicide while the Ge is expelled. The expelled germanium creates agglomeration and increases the resistance of the contacts. This increase in series resistance offsets the benefits of the extra drive current from the heterostructure, and negates the advantages of the structure.

Ti and Ni can form phases in which the Ge is not rejected severely, thus allowing the formation of a good contact. Co is much more problematic. However, as discussed above for the problem of Si removal, a protective layer(s) at the device epitaxy stage can be applied instead of optimizing the SiGe-metal reaction. For example, the strained Si that will become the surface channel can be coated with a high-Ge-content SiGe alloy (higher Ge content than the initial relaxed SiGe), followed by strained Si. Two approaches are possible using these surface contact layers. Both methods introduce thick Si at the surface and allow the conventional silicide technology to be practiced without encountering the problems with SiGe-metal reactions.

The first approach, shown on a surface channel heterostructure 900 in FIG. 9A, uses a Ge-rich layer 906 thin enough that it is substantially strained. The layer 906 is provided on a strained Si channel layer 904 and relaxed SiGe layer 902. In this case, if a subsequent Si layer 908 is beyond the critical thickness, the compressive Ge-rich layer 906 acts as a barrier to dislocations entering the strained Si channel 904. This barrier is beneficial since dislocations do not adversely affect the silicide process; thus, their presence in the subsequent Si layer 908 is of no consequence. However, if the dislocations were to penetrate to the channel, there would be adverse effects on the device.

A second approach, shown in FIG. 9B, is to allow a Ge-rich layer 910 to intentionally exceed the critical thickness, thereby causing substantial relaxation in the Ge-rich layer. In this scenario, an arbitrarily thick Si layer 912 can be applied on top of the relaxed Ge-rich layer. This layer will contain more defects than the strained channel, but the defects play no role in device operation since this Si is relevant only in the silicide reaction. In both cases, the process is free from the metal-SiGe reaction concerns, since the metal will react with Si-only.

Once the silicide contacts have been formed, the rest of the sequence is a standard Si CMOS process flow, except that the thermal budget is carefully monitored since, for example, the silicide-germanicide (if that option is used) typically cannot tolerate as high a temperature as the conventional silicide. A major advantage of using Si/SiGe FET heterostructures to achieve enhanced performance is the compatibility with conventional Si techniques. Many of the processes are identical to Si CMOS processing, and once the front-end of the process, i.e., the processing of the Si/SiGe heterostructure, is complete, the entire back-end process is uninfluenced by the fact that Si/SiGe lies below.

Even though the starting heterostructure for the buried channel device is different

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from that of the surface channel device, its process flow is very similar to the surface channel flow shown in FIGs. 7A-7D. FIG. 10 is a schematic block diagram of a buried channel MOSFET structure 1000 after the device isolation oxide 1016 has been formed using a SiN mask 1014. In this case, the strained channel 1002 on a first SiGe layer 1010 is separated from the surface by the growth of another SiGe layer 1004, followed by another Si layer 1006. This Si layer is needed for the gate oxide 1008 since gate-oxide formation on SiGe produces a very high interface state density, thus creating non-ideal MOSFETs. One consequence of this Si layer, is that if it is too thick, a substantial portion of the Si layer will remain after the gate oxidation. Carriers can populate this residual Si layer, creating a surface channel in parallel with the desired buried channel and leading to deleterious device properties. Thus, the surface layer Si must be kept as thin as possible, typically less than 50Å and ideally in the range of 5-15Å.

Another added feature that is necessary for a buried channel device is the supply layer implant. The field experienced in the vertical direction when the device is turned on is strong enough to pull carriers from the buried channel 1002 and force them to populate a Si channel 1006 near the Si/SiO₂ interface 1012, thus destroying any advantage of the buried channel. Thus, a supply layer of dopant must be introduced either in the layer 1004 between the buried channel and the top Si layer 1006, or below the buried channel in the underlying SiGe 1010. In this way, the device is forced on with little or no applied voltage, and turned off by applying a voltage (depletion mode device).

FIG. 11 is a schematic flow of the process, for any heterostructure FET device deposited on relaxed SiGe, in accordance with the invention. The main process steps are shown in the boxes, and optional steps or comments are shown in the circles. The first three steps (1100,1102,1104) describe the fabrication of the strained silicon heterostructure. The sequence includes production of relaxed SiGe on Si, planarization of the SiGe, and regrowth of the device layers. Once the strained heterostructure is complete (1106), MOS fabrication begins with device isolation (1112) using either STI (1110) or LOCOS (1108). Before proceeding to the gate oxidation, buried channel devices undergo a supply and threshold implant (1114), and any protective layers applied to either a buried or surface channel heterostructure must be selectively removed (1116). The processing sequence after the gate oxidation (1118) is similar to conventional Si CMOS processing. These steps include gate deposition, doping, and definition (1120), self-aligned shallow source-drain implant (1122), spacer formation (1124), self-aligned deep source-drain implant (1126), salicide formation (1128), and pad isolation via metal deposition and etch

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(1130). The steps requiring significant alteration have been discussed.

One particular advantage of the process of FIG. 11 is that it enables the use of surface channel and buried channel devices on the same platform. Consider FIGs. 12A-12D and FIGs. 13A-13D, which show a universal substrate layer configuration and a process that leads to the co-habitation of surface and buried channel MOSFETs on the same chip. The universal substrate is one in which both surface channel and buried channel devices can be fabricated. There are two possibilities in fabricating the surface channel device in this sequence, shown in FIGs. 12 and 13. The process flows for combining surface and buried channel are similar to the previous process described in FIG. 7. Therefore, only the critical steps involved in exposing the proper gate areas are shown in FIGs. 12 and 13.

FIGs. 12A and 13A depict the same basic heterostructure 1200,1300 for integrating surface channel and buried channel devices. There is a surface strained Si layer 1202,1302, a SiGe spacer layer 1204,1304, a buried strained Si layer 1206,1306, and a relaxed platform of SiGe 1208,1308. Two strained Si layers are necessary because the buried channel MOSFET requires a surface Si layer to form the gate oxide and a buried Si layer to form the device channel. The figures also show a device isolation region 1210 that separates the buried channel device area 1212,1312 from the surface channel device area 1214,1314.

Unlike the buried channel device, a surface channel MOSFET only requires one strained Si layer. As a result, the surface channel MOSFET can be fabricated either in the top strained Si layer, as shown in FIGs. 12B-12D, or the buried Si layer channel, as shown in FIGs. 13B-13D. FIG. 12B is a schematic diagram of a surface channel gate oxidation 1216 in the top Si layer 1202. In this scenario, a thicker top Si layer is desired, since after oxidation, a residual strained Si layer must be present to form the channel. FIG. 12B also shows a possible position for the buried channel supply implant 1218, which is usually implanted before the buried channel gate oxide is grown. Since the top Si layer is optimized for the surface channel device, it may be necessary to strip some of the top strained Si in the regions 1220 where buried channel devices are being created, as shown in FIG. 12C. This removal is necessary in order to minimize the surface Si thickness after gate oxide 1222 formation (FIG. 12D), and thus avoid the formation of a parallel device channel.

When a surface channel MOSFET is formed in the buried strained Si layer, the top strained Si layer can be thin, i.e., designed optimally for the buried channel MOSFET. In FIG. 13B, the top strained Si and SiGe layers are removed in the region 1312 where the

surface channel MOSFETs are formed. Because Si and SiGe have different properties, a range of selective removal techniques can be used, such as wet or dry chemical etching. Selective oxidation can also be used since SiGe oxidizes at much higher rates than Si, especially under wet oxidation conditions. FIG. 13C shows the gate oxidation 1314 of the surface channel device as well as the supply layer implant 1316 for the buried channel device. Finally, FIG. 13D shows the position of the buried channel gate oxide 1318. No thinning of the top Si layer is required prior to the oxidation since the epitaxial thickness is optimized for the buried channel device. Subsequent to these initial steps, the processing for each device proceeds as previously described.

Another key step in the process is the use of a localized implant to create the supply layer needed in the buried channel device. In a MOSFET structure, when the channel is turned on, large vertical fields are present that bring carriers to the surface. The band offset between the Si and SiGe that confines the electrons in the buried strained Si layer is not large enough to prevent carriers from being pulled out of the buried channel. Thus, at first, the buried channel MOSFET would appear useless. However, if enough charge were present in the top SiGe layer, the MOSFET would become a depletion-mode device, i.e. normally on and requiring bias to turn off the channel. In the surface/buried channel device platform, a supply layer implant can be created in the regions where the buried channel will be fabricated, thus easing process integration. If for some reason the supply layer implant is not possible, note that the process shown in FIG. 11 in which the surface channel is created on the buried Si layer is an acceptable process, since the dopant can be introduced into the top SiGe layer during epitaxial growth. The supply layer is then removed from the surface channel MOSFET areas when the top SiGe and strained Si layers are selectively etched away.

In the processes described in FIGs. 10, 12 and 13, it is assumed that the desire is to fabricate a buried channel MOSFET. If the oxide of the buried channel device is removed, one can form a buried channel device with a metal gate (termed a MODFET or HEMT). The advantage of this device is that the transconductance can be much higher since there is a decrease in capacitance due to the missing oxide. However, there are two disadvantages to using this device. First, all thermal processes after gate definition have to be extremely low temperature, otherwise the metal will react with the semiconductor, forming an alloyed gate with a very low, or non-existent, barrier. Related to this issue is the second disadvantage. Due to the low thermal budget, the source and drain formation and contacts are typically done before the gate definition. Inverting these steps prevents the gate from being self-aligned to the source and drain, thus increasing the series resistance between the

gate and the source and drain. Therefore, with a carefully designed buried channel MOSFET, the self-aligned nature can be a great advantage in device performance. Another benefit of the MOSFET structure is that the gate leakage is very low.

The combination of buried n-channel structures with n and p type surface channel MOSFETs has been emphasized heretofore. It is important to also emphasize that in buried n-channel devices as well as in surface channel devices, the channels need not be pure Si. $\text{Si}_{1-y}\text{Ge}_y$ channels can be used to increase the stability during processing. FIGs. 14A and 14B are schematic diagrams of surface 1400 and buried 1450 channel devices with $\text{Si}_{1-y}\text{Ge}_y$ channels 1402 on a relaxed $\text{Si}_{1-z}\text{Ge}_z$ layer 1404. The devices are shown after salicidation and thus contain a poly-Si gate 1410, gate oxide 1408, silicide regions 1412, spacers 1414, and doped regions 1416. In the surface channel device 1400, a thin layer 1406 of Si must be deposited onto the $\text{Si}_{1-y}\text{Ge}_y$ layer 1402 to form the gate oxide 1408, as previously described for buried channel devices. In the buried $\text{Si}_{1-y}\text{Ge}_y$ channel device 1450, the device layer sequence is unchanged and consists of a buried strained channel 1402, a SiGe spacer layer 1418, and a surface Si layer 1420 for oxidation.

To maintain tensile strain in the channel of an nMOS device, the lattice constant of the channel layer must be less than that of the relaxed SiGe layer, i.e., y must be less than z . Since n-channel devices are sensitive to alloy scattering, the highest mobilities result when the Ge concentration in the channel is low. In order to have strain on this channel layer at a reasonable critical thickness, the underlying SiGe should have a Ge concentration in the range of 10-50%.

Experimental data indicates that p channels are less sensitive to alloy scattering. Thus, surface MOSFETs with alloy channels are also possible. In addition, the buried channel devices can be p-channel devices simply by having the Ge concentration in the channel, y , greater than the Ge concentration in the relaxed SiGe alloy, z , and by switching the supply dopant from n-type to p-type. This configuration can be used to form Ge channel devices when $y = 1$ and $0.5 < z < 0.9$.

With the ability to mix enhancement mode surface channel devices (n and p channel, through implants as in typical Si CMOS technology) and depletion-mode buried channel MOSFETs and MODFETs, it is possible to create highly integrated digital/analog systems. The enhancement mode devices can be fabricated into high performance CMOS, and the regions of an analog circuit requiring the high performance low-noise depletion mode device can be fabricated in the buried channel regions. Thus, it is possible to construct optimal communication stages, digital processing stages, etc. on a single

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platform. These different regions are connected electrically in the backend of the Si CMOS chip, just as transistors are connected by the back-end technology today. Thus, the only changes to the CMOS process are some parameters in the processes in the fabrication facility, and the new material, but otherwise, the entire manufacturing process
5 is transparent to the change. Thus, the economics favor such a platform for integrated Si CMOS systems on chip.

Although the present invention has been shown and described with respect to several preferred embodiments thereof, various changes, omissions and additions to the form and detail thereof, may be made therein, without departing from the spirit and
10 scope of the invention.

What is claimed is:

CLAIMS

- 1 1. A surface channel MOSFET comprising:
2 a relaxed planarized SiGe layer on a substrate;
3 a regrown $\text{Si}_{1-x}\text{Ge}_x$ layer with thickness h ;
4 a Si channel layer;
5 a gate dielectric;
6 a polycrystalline semiconductor layer; and
7 a highly conductive gate layer.
- 1 2. The MOSFET of claim 1, wherein h is approximately 0.
- 1 3. The MOSFET of claim 1, wherein the substrate comprises relaxed graded
2 composition SiGe layers on Si.
- 1 4. The MOSFET of claim 1, wherein the substrate comprises Si.
- 1 5. The MOSFET of claim 1, wherein the substrate comprises Si with a layer of
2 SiO_2 .
- 1 6. A surface channel MOSFET comprising:
2 a relaxed planarized SiGe layer on a substrate;
3 a regrown $\text{Si}_{1-x}\text{Ge}_x$ layer with thickness h ;
4 a Ge channel layer;
5 a Si layer;
6 a gate dielectric;
7 a polycrystalline semiconductor layer; and
8 a highly conductive gate layer.
- 1 7. The MOSFET of claim 6, wherein h is approximately 0.
- 1 8. The MOSFET of claim 6, wherein the thickness of the Si layer is less than
2 5nm.

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1 9. The MOSFET of claim 6, wherein the substrate comprises relaxed
2 graded composition SiGe layers on Si.

1 10. The MOSFET of claim 6, wherein the substrate comprises Si.

1 11. The MOSFET of claim 6, wherein the substrate comprises Si with a layer
2 of SiO₂.

1 12. A buried channel MOSFET comprising:
2 a relaxed planarized SiGe layer on a substrate;
3 a regrown Si_{1-x}Ge_x layer with thickness h;
4 a Si channel layer;
5 a Si_{1-y}Ge_y layer;
6 a second Si layer;
7 a gate dielectric;
8 a polycrystalline semiconductor layer; and
9 a highly conductive gate metal layer.

1 13. The MOSFET of claim 12, wherein h is approximately 0.

1 14. The MOSFET of claim 12, wherein the thickness of the second Si layer is
2 less than 5nm.

1 15. The MOSFET of claim 12, wherein supply layer dopants are located in the
2 Si_{1-y}Ge_y layer.

1 16. The MOSFET of claim 15, wherein the supply layer dopants are implanted.

1 17. The MOSFET of claim 12, wherein the supply layer dopants are located
2 below the Si channel layer.

1 18. The MOSFET of claim 17, wherein the supply layer dopants are implanted.

1 19. The MOSFET of claim 12, wherein the substrate comprises relaxed graded
2 composition SiGe layers on Si.

1 20. The MOSFET of claim 12, wherein the substrate comprises Si.

1 21. The MOSFET of claim 12, wherein the substrate comprises Si with a layer

2 of SiO₂.

1 22. A buried channel FET comprising:
2 a relaxed planarized SiGe layer on a substrate;
3 a regrown Si_{1-x}Ge_x layer with thickness h;
4 a Si channel layer;
5 a Si_{1-y}Ge_y layer;
6 a second Si layer; and
7 a highly conductive gate layer.

1 23. The FET of claim 22, wherein h is approximately 0.

1 24. The FET of claim 22, wherein the thickness of the second Si layer is less
2 than 5nm.

1 25. The FET of claim 22, wherein supply layer dopants are located in the Si₁₋
2 _yGe_y layer.

1 26. The FET of claim 25, wherein the supply layer dopants are implanted.

1 27. The FET of claim 22, wherein the supply layer dopants are located below
2 the Si channel layer.

1 28. The FET of claim 27, wherein the supply layer dopants are implanted.

1 29. The FET of claim 22, wherein the substrate comprises relaxed graded
2 composition SiGe layers on Si.

1 30. The FET of claim 22, wherein the substrate comprises Si.

1 31. The FET of claim 22, wherein the substrate comprises Si with a layer of
2 SiO₂.

1 32. A method of fabricating a surface channel MOSFET comprising:
2 providing a relaxed SiGe layer on a substrate;
3 planarizing said relaxed SiGe layer;
4 providing a regrown Si_{1-x}Ge_x layer with thickness h on said planarized relaxed
5 SiGe layer;

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6 providing a Si channel layer on said regrown $\text{Si}_{1-x}\text{Ge}_x$ layer;
7 providing a gate dielectric on said Si channel layer;
8 providing a polycrystalline semiconductor layer on said gate dielectric; and
9 providing a highly conductive gate layer on said polycrystalline semiconductor
10 layer.

1 33. The method of claim 32, wherein h is approximately 0.

1 34. The method of claim 32, wherein the substrate comprises relaxed graded
2 composition SiGe layers on Si.

1 35. The method of claim 32, wherein the substrate comprises Si.

1 36. The method of claim 32, wherein the substrate comprises Si with a layer of
2 SiO_2 .

1 37. A method of fabricating a surface channel MOSFET comprising:
2 providing a relaxed SiGe layer on a substrate;
3 planarizing said relaxed SiGe layer;
4 providing a regrown $\text{Si}_{1-x}\text{Ge}_x$ layer with thickness h on said planarized relaxed
5 SiGe layer;
6 providing a Ge channel layer on said regrown $\text{Si}_{1-x}\text{Ge}_x$ layer;
7 providing a Si layer on said Ge channel layer;
8 providing a gate dielectric on said Si layer;
9 a polycrystalline semiconductor layer; and
10 a highly conductive gate layer.

1 38. The method of claim 37, wherein h is approximately 0.

1 39. The method of claim 37, wherein the thickness of the Si layer is less than
2 5nm.

1 40. The method of claim 37, wherein the substrate comprises relaxed graded
2 composition SiGe layers on Si.

1 41. The method of claim 37, wherein the substrate comprises Si.

1 42. The method of claim 37, wherein the substrate comprises Si with a layer of

2 SiO₂.

1 43. A method of fabricating a buried channel MOSFET comprising:
2 providing a relaxed SiGe layer on a substrate;
3 planarizing said relaxed SiGe layer;
4 providing a regrown Si_{1-x}Ge_x layer with thickness h on said planarized relaxed
5 SiGe layer;
6 providing a Si channel layer on said regrown Si_{1-x}Ge_x layer;
7 providing a Si_{1-y}Ge_y layer on said Si channel layer;
8 providing a Si layer on said Si_{1-y}Ge_y layer;
9 providing a gate dielectric on said Si layer;
10 providing a polycrystalline semiconductor layer on said gate dielectric; and
11 providing a highly conductive gate metal layer on said polycrystalline
12 semiconductor layer.

1 44. The method of claim 43, wherein h is approximately 0.

1 45. The method of claim 43, wherein the thickness of the Si layer is less than
2 5nm.

1 46. The method of claim 43, wherein supply layer dopants are located in the
2 Si_{1-y}Ge_y layer.

1 47. The method of claim 46, wherein the supply layer dopants are implanted.

1 48. The method of claim 43, wherein the supply layer dopants are located
2 below the Si channel layer.

1 49. The method of claim 48, wherein the supply layer dopants are implanted.

1 50. The method of claim 43, wherein the substrate comprises relaxed graded
2 composition SiGe layers on Si.

1 51. The method of claim 43, wherein the substrate comprises Si.

1 52. The method of claim 43, wherein the substrate comprises Si with a layer of
2 SiO₂.

- 1 53. A method of fabricating a buried channel FET comprising:
2 providing a relaxed SiGe layer on a substrate;
3 planarizing said relaxed SiGe layer;
4 providing a regrown $\text{Si}_{1-x}\text{Ge}_x$ layer with thickness h on said planarized relaxed
5 SiGe layer;
6 providing a Si channel layer on said regrown $\text{Si}_{1-x}\text{Ge}_x$ layer;
7 providing a $\text{Si}_{1-y}\text{Ge}_y$ layer on said Si channel layer;
8 providing a Si layer on said $\text{Si}_{1-y}\text{Ge}_y$ layer; and
9 providing a highly conductive gate layer on said Si layer.
- 1 54. The method of claim 53, wherein h is approximately 0.
- 1 55. The method of claim 53, wherein the thickness of the second Si layer is less
2 than 5nm.
- 1 56. The method of claim 53, wherein supply layer dopants are located in the
2 $\text{Si}_{1-y}\text{Ge}_y$ layer.
- 1 57. The method of claim 56, wherein the supply layer dopants are implanted.
- 1 58. The method of claim 53, wherein the supply layer dopants are located
2 below the Si channel layer.
- 1 59. The method of claim 58, wherein the supply layer dopants are implanted.
- 1 60. The method of claim 53, wherein the substrate comprises relaxed graded
2 composition SiGe layers on Si.
- 1 61. The method of claim 53, wherein the substrate comprises Si.
- 1 62. The method of claim 53, wherein the substrate comprises Si with a layer of
2 SiO_2 .
- 1 63. A method of fabricating a surface channel MOSFET on a heterostructure,
2 said heterostructure including a planarized relaxed SiGe layer on a substrate, a regrown
3 $\text{Si}_{1-x}\text{Ge}_x$ layer with thickness h on said planarized relaxed SiGe layer, and a Si channel
4 layer on said regrown $\text{Si}_{1-x}\text{Ge}_x$ layer, said method comprising:
5 providing a gate dielectric on said Si channel layer;

6 providing a polycrystalline semiconductor layer on said gate dielectric;
7 and
8 providing a highly conductive gate layer on said polycrystalline semiconductor
9 layer.

1 64. The method of claim 63, wherein h is approximately 0.

1 65. The method of claim 63, wherein the substrate comprises relaxed graded
2 composition SiGe layers on Si.

1 66. The method of claim 63, wherein the substrate comprises Si.

1 67. The method of claim 63, wherein the substrate comprises Si with a layer of
2 SiO₂.

1 68. A method of fabricating a surface channel MOSFET on a heterostructure,
2 said heterostructure including a planarized relaxed SiGe layer on a substrate, a regrown
3 Si_{1-x}Ge_x layer with thickness h on said planarized relaxed SiGe layer, a Ge channel
4 layer on said regrown Si_{1-x}Ge_x layer, and a Si layer on said Ge channel layer, said
5 method comprising:

6 providing a gate dielectric on said Si layer;
7 providing a polycrystalline semiconductor layer; and
8 providing a highly conductive gate layer.

1 69. The method of claim 68, wherein h is approximately 0.

1 70. The method of claim 68, wherein the thickness of the Si layer is less than
2 5nm.

1 71. The method of claim 68, wherein the substrate comprises relaxed graded
2 composition SiGe layers on Si.

1 72. The method of claim 68, wherein the substrate comprises Si.

1 73. The method of claim 68, wherein the substrate comprises Si with a layer of
2 SiO₂.

1 74. A method of fabricating a buried channel MOSFET on a
2 heterostructure, said heterostructure including a planarized relaxed SiGe layer on a
3 substrate, a regrown $\text{Si}_{1-x}\text{Ge}_x$ layer with thickness h on said planarized relaxed SiGe layer,
4 a Si channel layer on said regrown $\text{Si}_{1-x}\text{Ge}_x$ layer, a $\text{Si}_{1-y}\text{Ge}_y$ layer on said Si channel layer,
5 and a Si layer on said $\text{Si}_{1-y}\text{Ge}_y$ layer, said method comprising:

6 providing a gate dielectric on said Si layer;
7 providing a polycrystalline semiconductor layer on said gate dielectric; and
8 providing a highly conductive gate metal layer on said polycrystalline
9 semiconductor layer.

1 75. The method of claim 74, wherein h is approximately 0.

1 76. The method of claim 74, wherein the thickness of the Si layer is less than
2 5nm.

1 77. The method of claim 74, wherein supply layer dopants are located in the
2 $\text{Si}_{1-y}\text{Ge}_y$ layer.

1 78. The method of claim 77, wherein the supply layer dopants are implanted.

1 79. The method of claim 74, wherein the supply layer dopants are located
2 below the Si channel layer.

1 80. The method of claim 79, wherein the supply layer dopants are implanted.

1 81. The method of claim 74, wherein the substrate comprises relaxed graded
2 composition SiGe layers on Si.

1 82. The method of claim 74, wherein the substrate comprises Si.

1 83. The method of claim 74, wherein the substrate comprises Si with a layer of
2 SiO_2 .

1 84. A method of fabricating a buried channel FET on a heterostructure, said
2 heterostructure including a planarized relaxed SiGe layer on a substrate, a regrown $\text{Si}_{1-x}\text{Ge}_x$
3 layer with thickness h on said planarized relaxed SiGe layer, a Si channel layer on said
4 regrown $\text{Si}_{1-x}\text{Ge}_x$ layer, a $\text{Si}_{1-y}\text{Ge}_y$ layer on said Si channel layer, and a Si layer on said $\text{Si}_{1-y}\text{Ge}_y$

5 $y\text{Ge}_y$ layer, said method comprising:

6 providing a highly conductive gate layer on said Si layer.

1 85. The method of claim 84, wherein h is approximately 0.

1 86. The method of claim 84, wherein the thickness of the second Si layer is less
2 than 5nm.

1 87. The method of claim 84, wherein supply layer dopants are located in the
2 $\text{Si}_{1-y}\text{Ge}_y$ layer.

1 88. The method of claim 87, wherein the supply layer dopants are implanted.

1 89. The method of claim 84, wherein the supply layer dopants are located
2 below the Si channel layer.

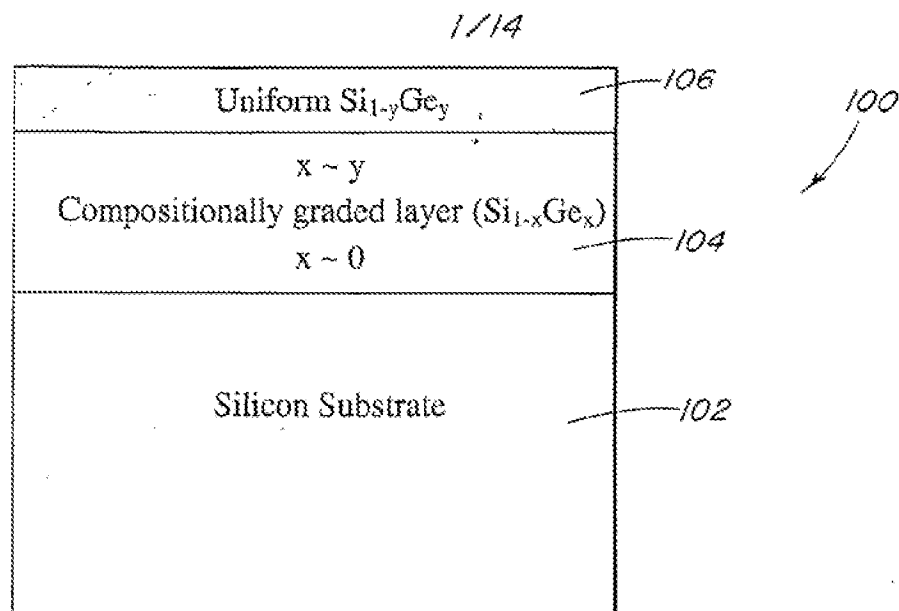
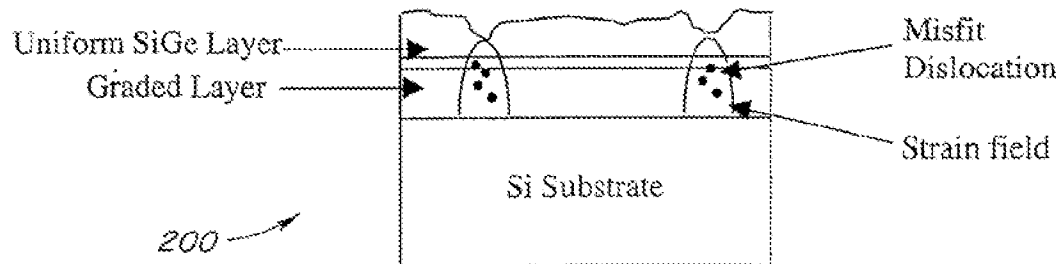
1 90. The method of claim 89, wherein the supply layer dopants are implanted.

1 91. The method of claim 84, wherein the substrate comprises relaxed graded
2 composition SiGe layers on Si.

1 92. The method of claim 84, wherein the substrate comprises Si.

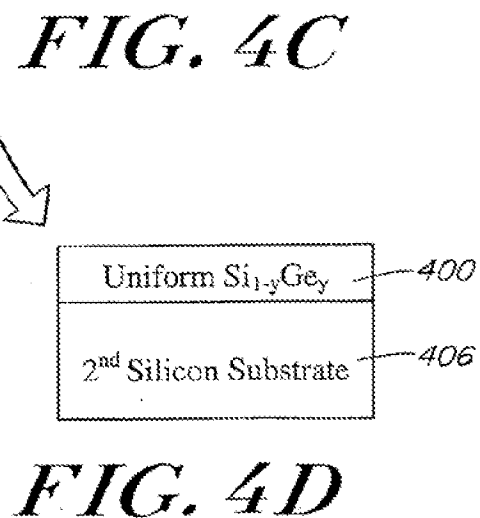
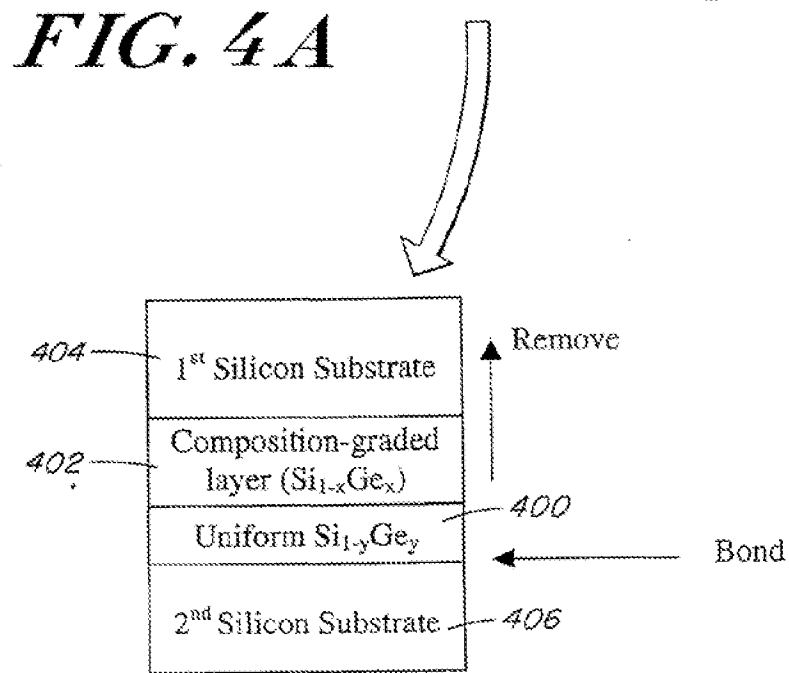
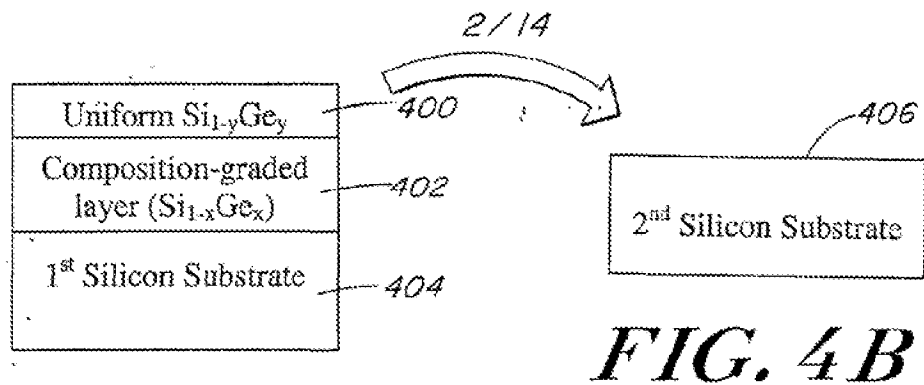
1 93. The method of claim 84, wherein the substrate comprises Si with a layer of
2 SiO_2 .

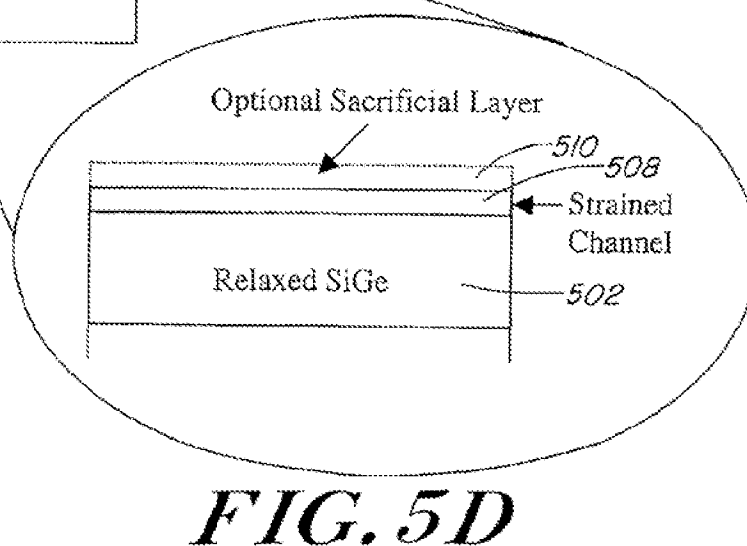
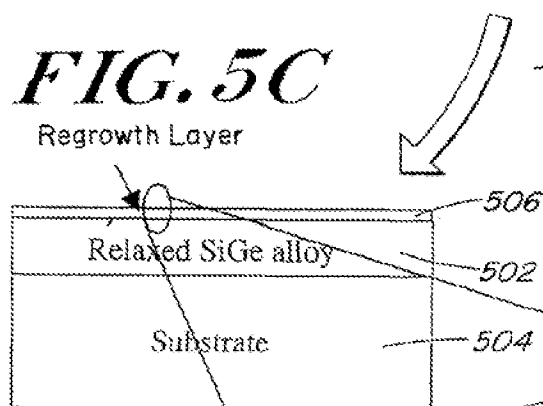
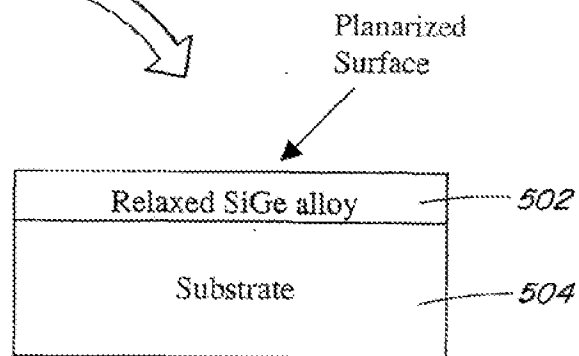
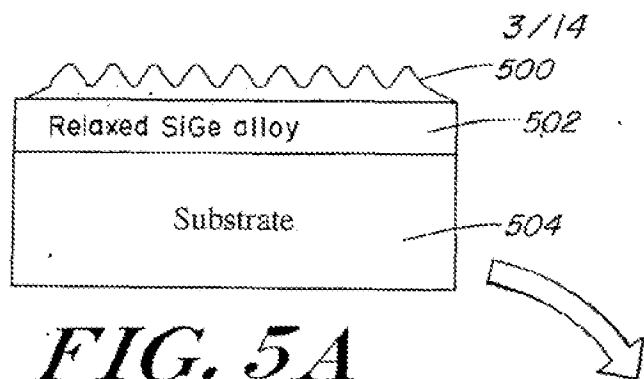
1 94. A method of fabricating a semiconductor structure comprising:
2 providing a relaxed $\text{Si}_{1-x}\text{Ge}_x$ layer on a substrate;
3 planarizing said relaxed $\text{Si}_{1-x}\text{Ge}_x$ layer;
4 depositing a heterostructure on said planarized relaxed $\text{Si}_{1-x}\text{Ge}_x$ layer including
5 at least one strained layer; and
6 configuring a semiconductor device on said heterostructure.

**FIG. 1****FIG. 2**

| Type of Surface | Average Roughness (nm) |
|---|---------------------------|
| As-grown graded composition relaxed SiGe | 7.9 |
| Planarized SiGe | 0.57 |
| Regrowth SiGe, lattice-matched | ~0.6 |
| Regrowth SiGe, slight mismatch, thickness = 1.5 μ m | 0.77 |

FIG. 3





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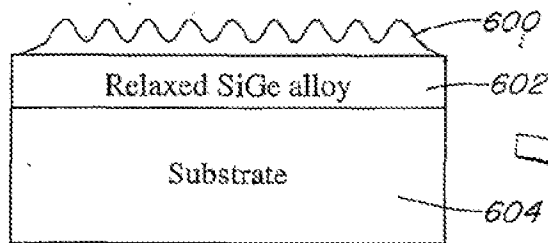


FIG. 6A

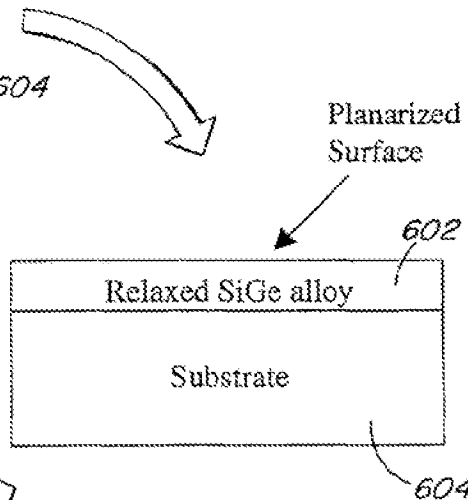


FIG. 6B

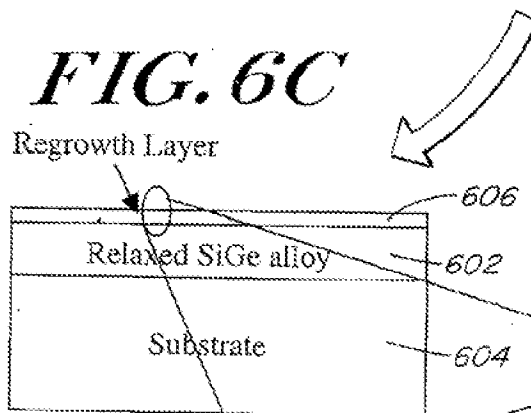


FIG. 6C

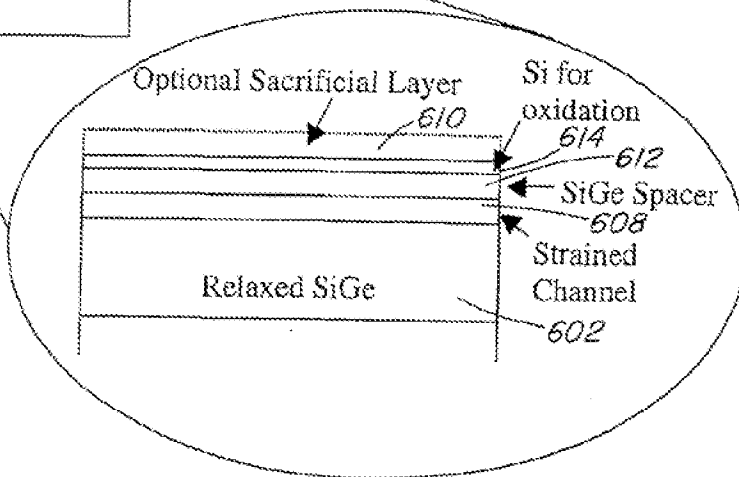
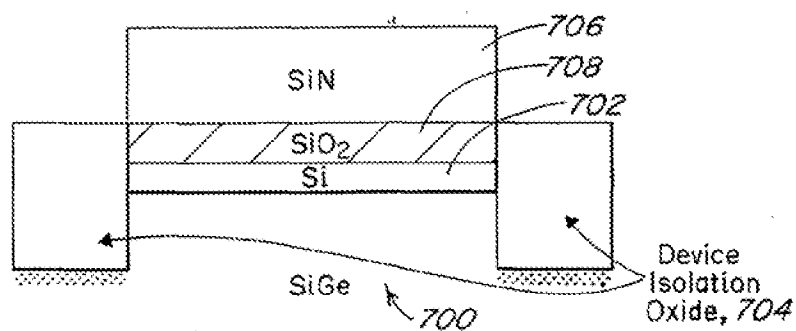
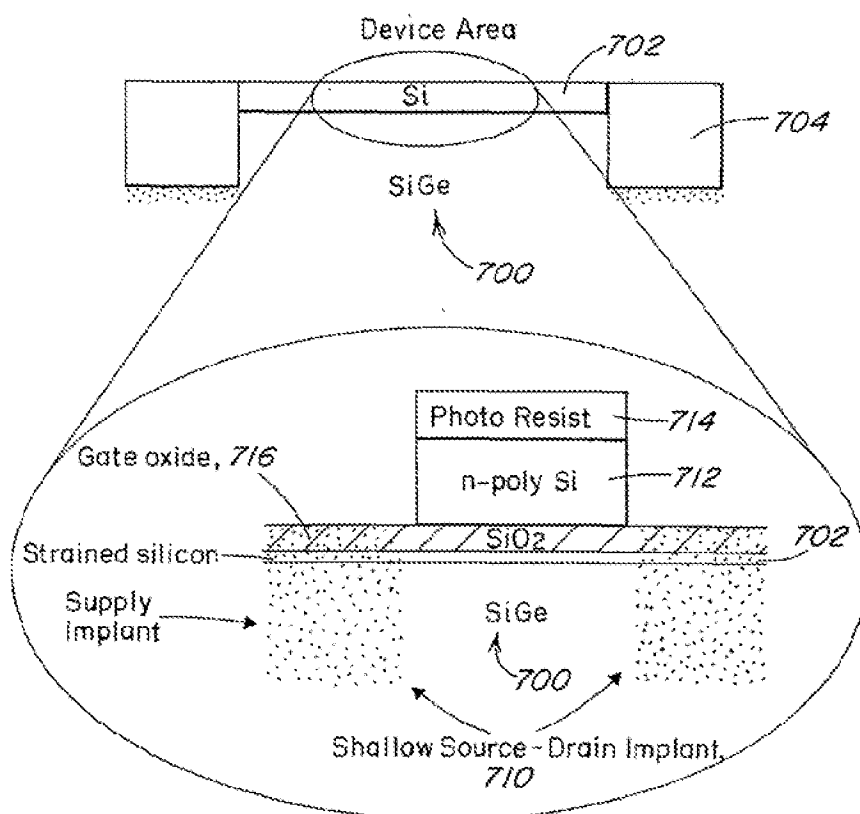
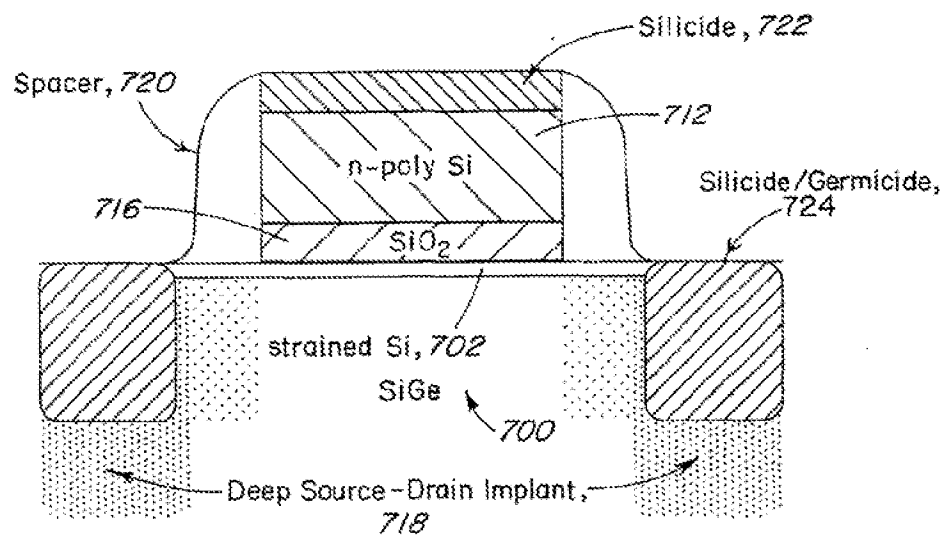
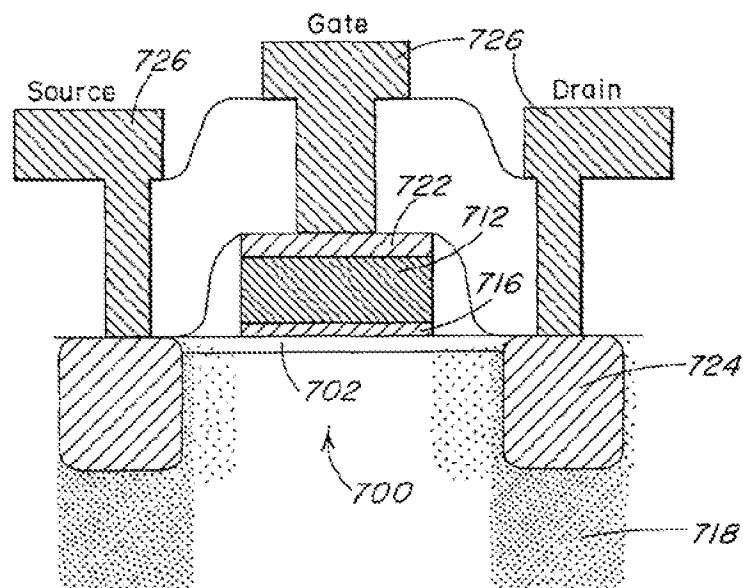


FIG. 6D

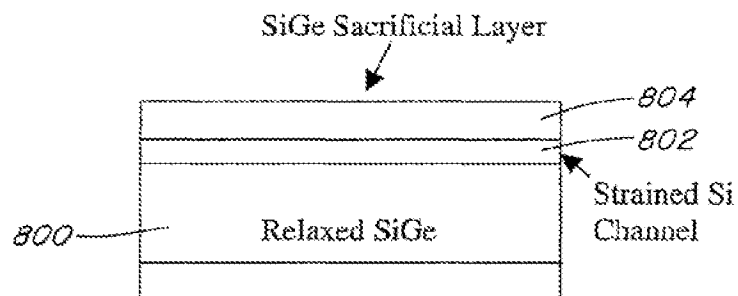
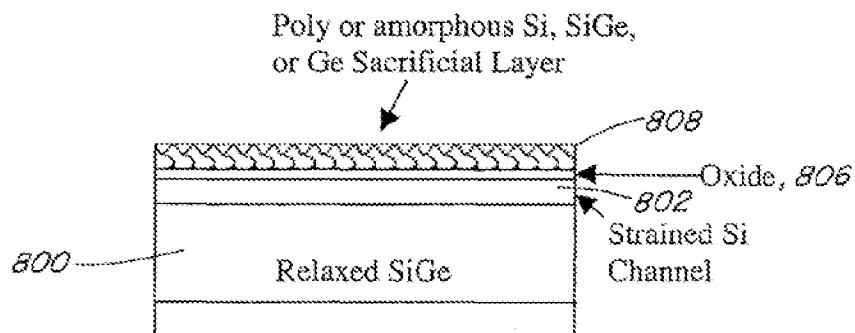
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**FIG. 7A****FIG. 7B**

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**FIG. 7C****FIG. 7D**

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**FIG. 8A****FIG. 8B**

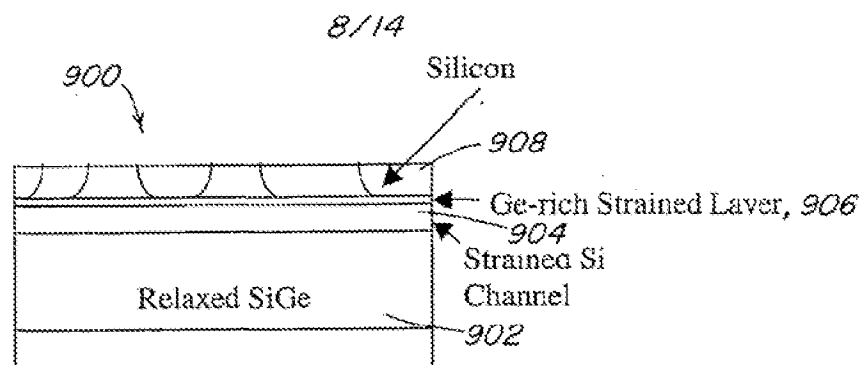


FIG. 9A

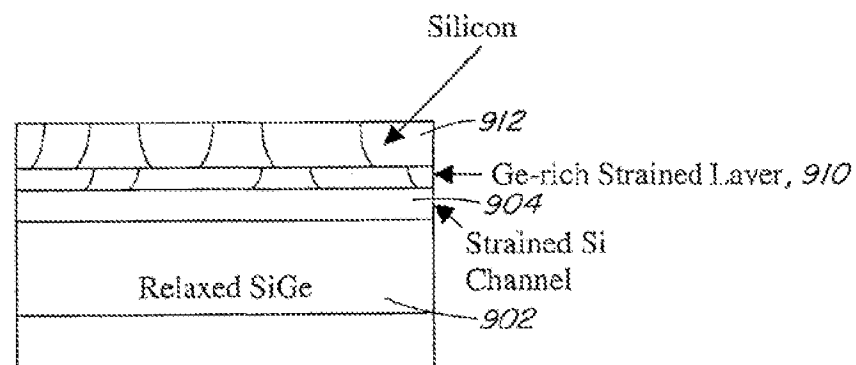


FIG. 9B

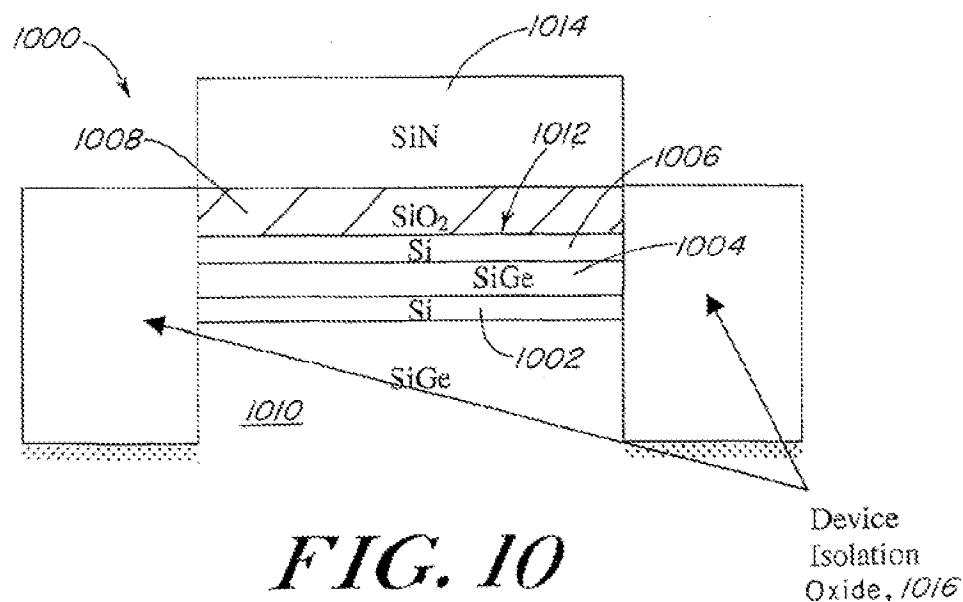
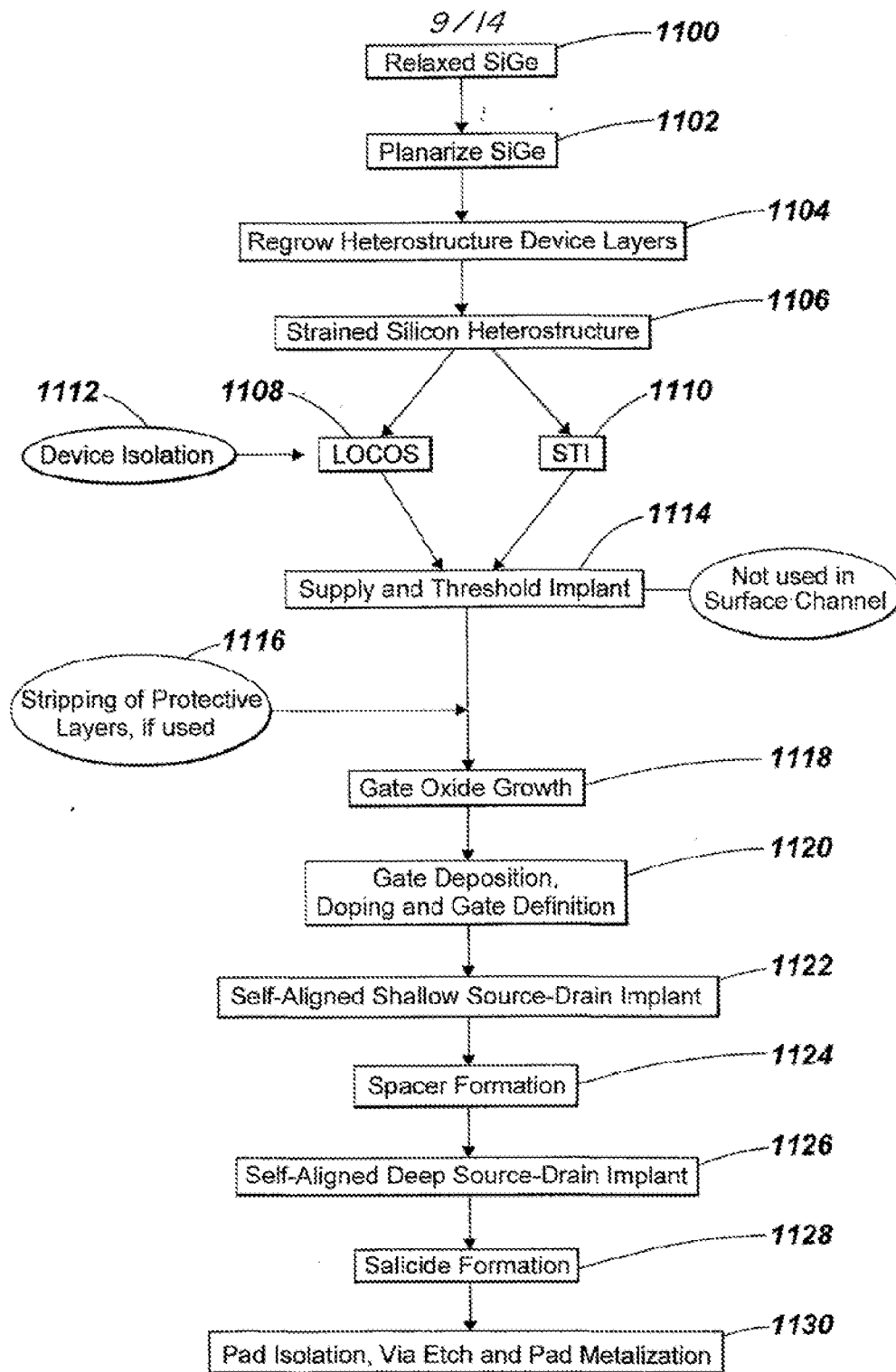


FIG. 10

**FIG. 11**

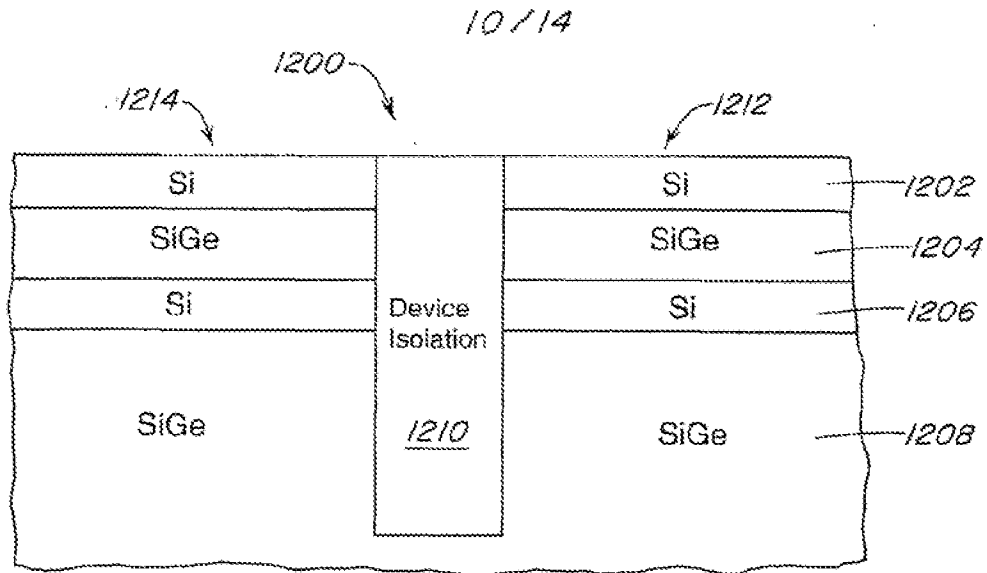


FIG. 12A

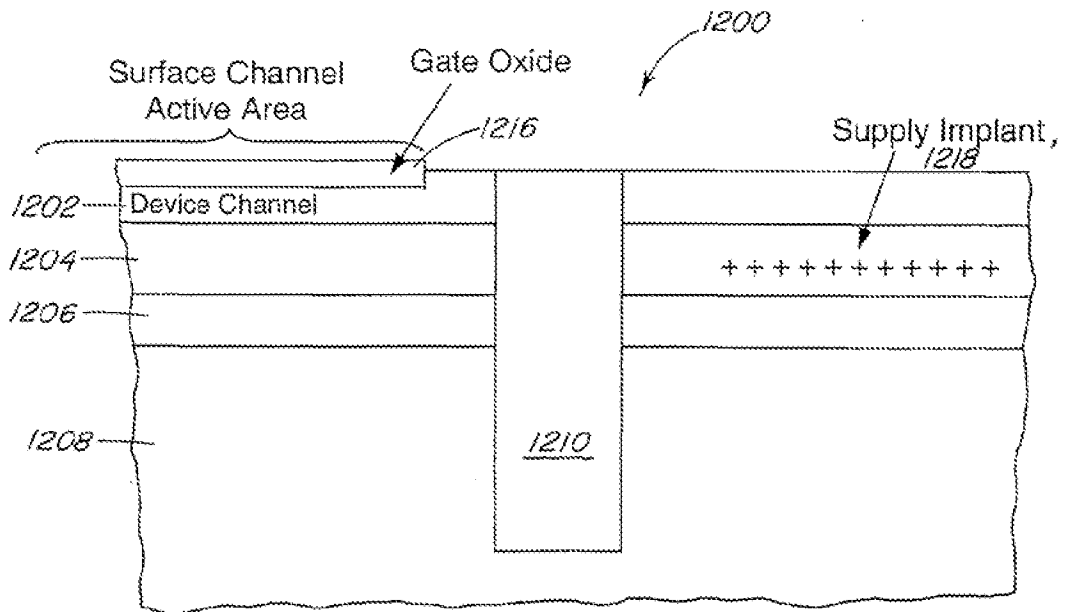


FIG. 12B

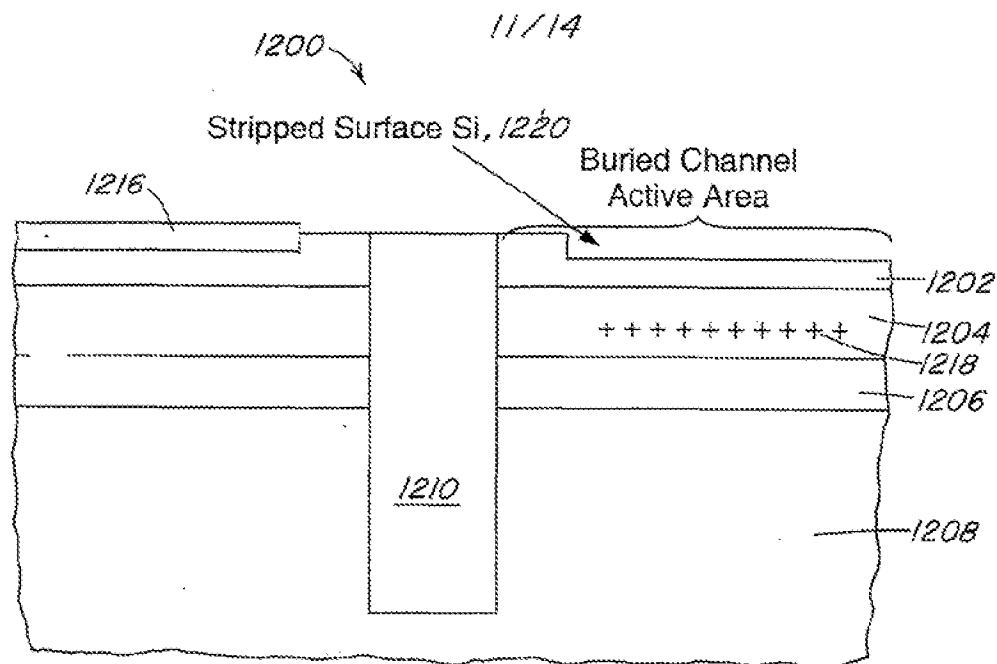


FIG. 12C

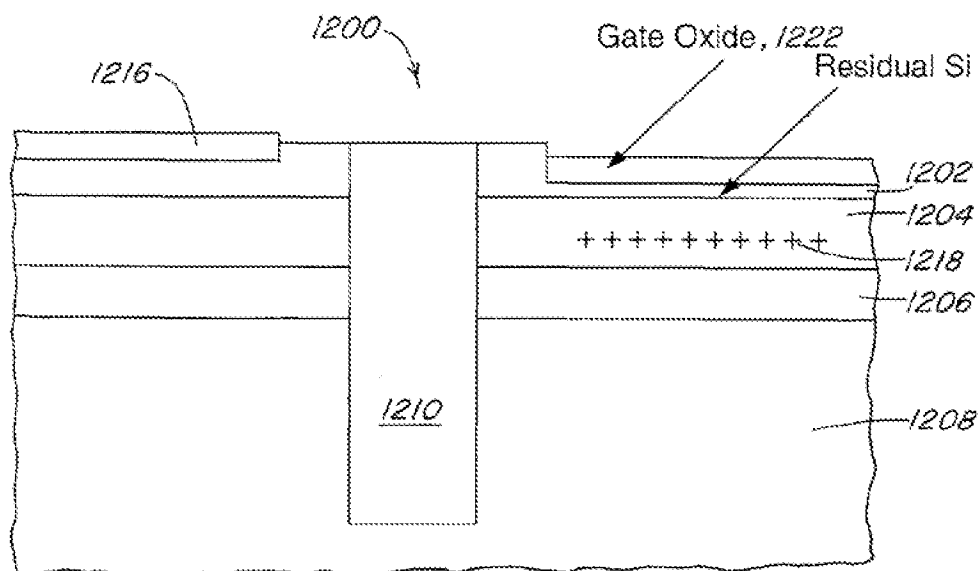
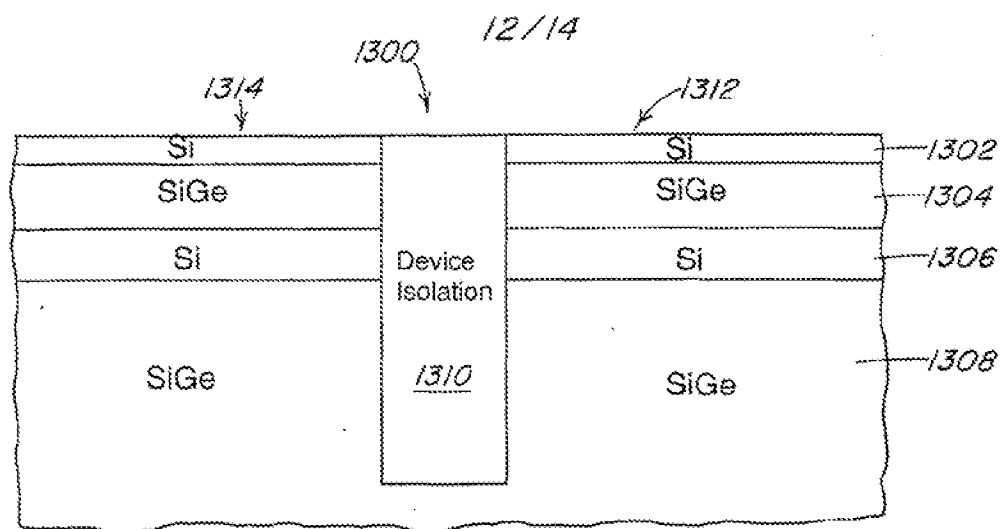
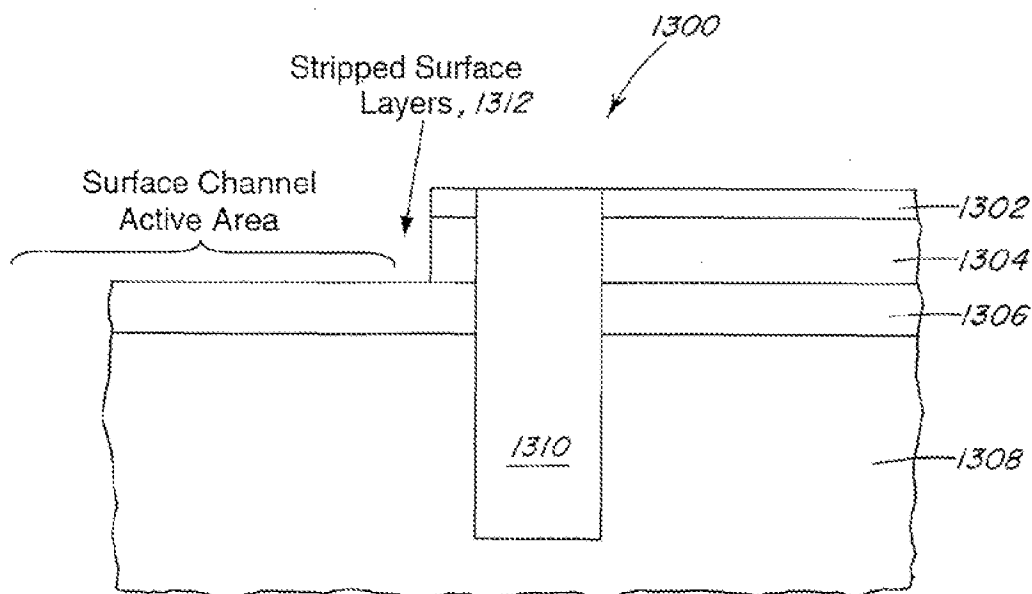


FIG. 12D

**FIG. 13A****FIG. 13B**

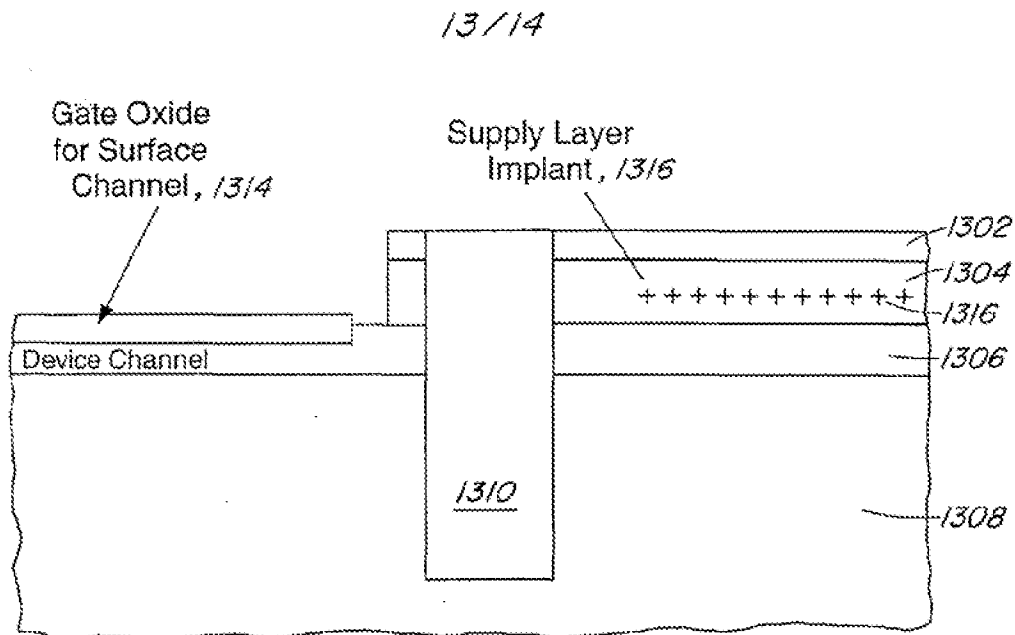


FIG. 13C

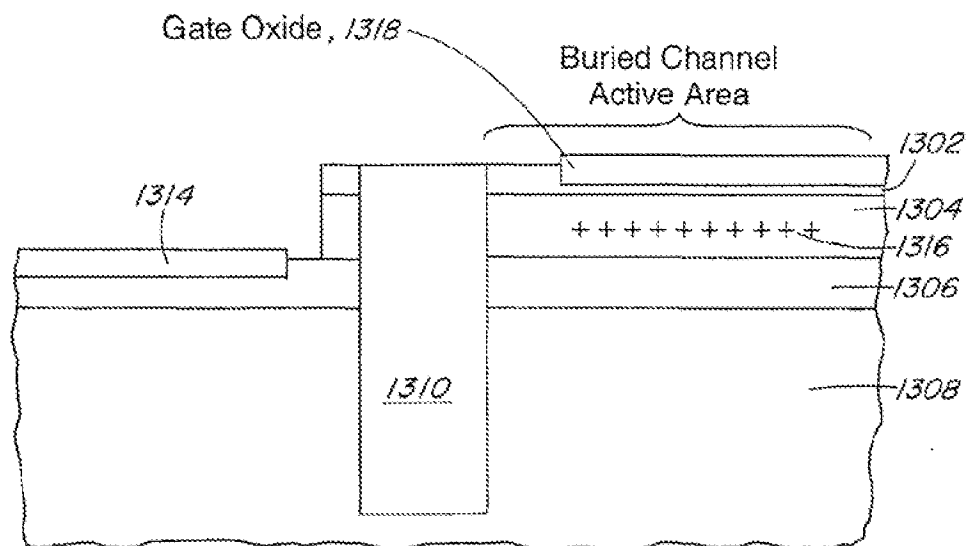
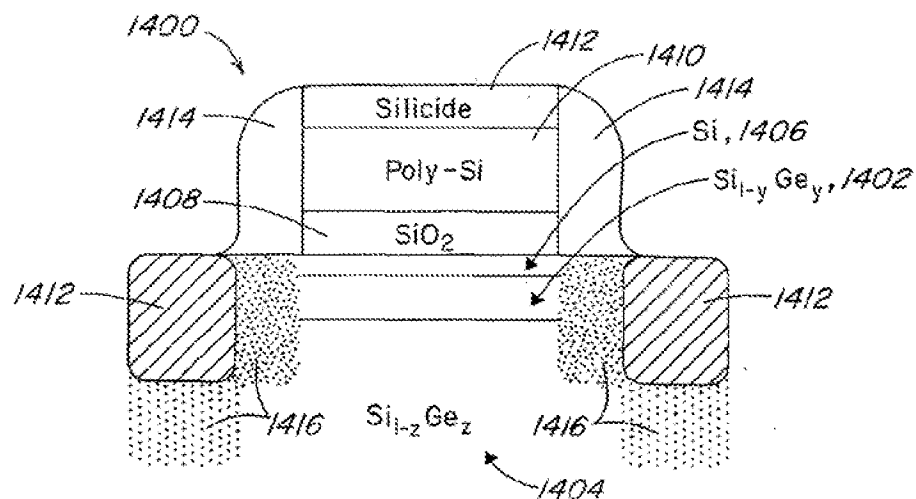
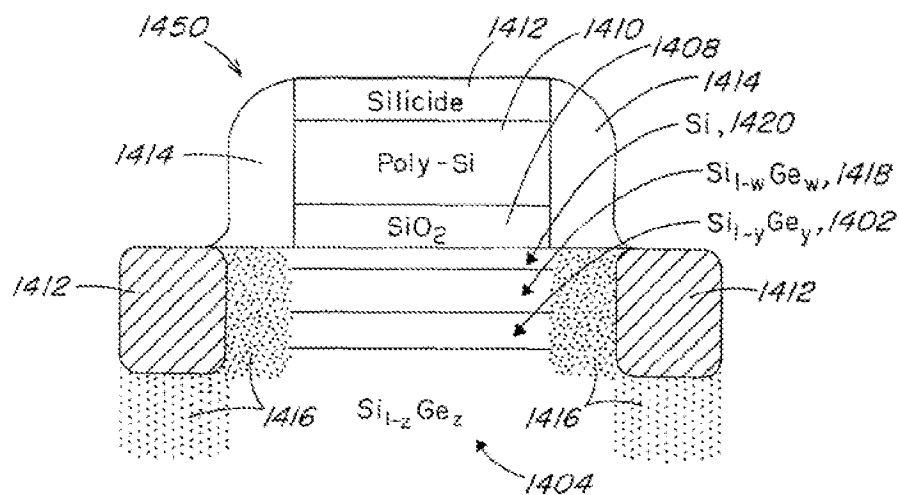


FIG. 13D

14/14

**FIG. 14A****FIG. 14B**

INTERNATIONAL SEARCH REPORT

International Application No.
PCT/US 02/03688

A. CLASSIFICATION OF SUBJECT MATTER

IPC 7 H01L29/10 H01L29/778 H01L21/335 H01L21/336 H01L29/80

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, COMPENDEX, INSPEC, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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| Y | MAITI K ET AL: "STRAINED-SI HETEROSTRUCTURE FIELD EFFECT TRANSISTORS" SEMICONDUCTOR SCIENCE AND TECHNOLOGY, INSTITUTE OF PHYSICS. LONDON, GB, vol. 13, no. 11, 1 November 1998 (1998-11-01), pages 1225-1246, XP000783138 ISSN: 0268-1242 page 1235 -page 1238; figures 13-18 -/- | 1-93 |

☒ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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Z document member of the same patent family

Date of the actual completion of the international search

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INTERNATIONAL SEARCH REPORT

International Application No.

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INTERNATIONAL SEARCH REPORT

International Application No.

PCT/US 02/03688

| C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT | | |
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| Category * | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
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Information on patent family members

International Application No.

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| Patent document cited in search report | | Publication date | Patent family member(s) | Publication date |
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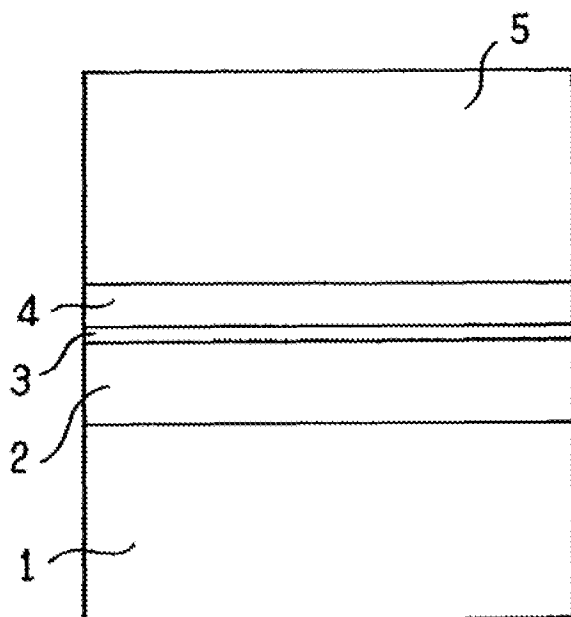
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- (21) International Application Number: PCT/IB2003/003497 (81) Designated States (national): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.
- (22) International Filing Date: 9 July 2003 (09.07.2003) (84) Designated States (regional): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).
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(54) Title: TRANSFER OF A THIN LAYER FROM A WAFER COMPRISING A BUFFER LAYER



(57) Abstract: Method of producing a structure comprising a thin layer of semiconductor material obtained from a wafer (10), the wafer (10) comprising a lattice parameter matching layer (2) comprising an upper layer of semiconductor material having a first lattice parameter, a film (3) of semiconductor material which has a nominal lattice parameter substantially different from the first lattice parameter and is strained by the matching layer (2), a relaxed layer (4) having a nominal lattice parameter substantially identical to the first lattice parameter, the method comprising transfer of the relaxed layer (4) and the strained film (3) to a receiving substrate (5). Structures produced according to one of the processes according to the invention.

WO 2004/006311 A2



For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

"TRANSFER OF A THIN LAYER FROM A WAFER COMPRISING A BUFFER LAYER"

The present invention relates to a transfer of thin layers from a wafer to a receiving substrate, in order to form structures such as a semiconductor-on-insulator structure, also called an SeOI (Semiconductor-on-insulator) structure.

A first object of a such transfer is usually to produce electronic structures whose active layer, that is to say the layer which comprises or which will comprise the electronic components, is particularly thin and particularly homogeneous through the thickness.

A second object of the transfer can also be to produce these structures by transferring the active layer onto a receiving substrate from a wafer comprising a buffer layer.

A third object of the transfer may be to provide the possibility of reusing part of the wafer, and especially at least part of the buffer layer, for another transfer.

The term "buffer layer" is understood to mean a layer intermediate between two crystallographic structures with different lattice parameters, having in the region of one of its faces a lattice parameter substantially identical to that of the first structure and in the region of its other face a lattice parameter substantially identical to that of the second structure.

Thus, a wafer may, for example, comprise a single-crystal silicon (also called Si) wafer on which a relaxed layer of silicon-germanium (also called SiGe) is produced by means of a buffer layer, despite the difference in lattice parameter existing between these two materials.

By "relaxed layer" it is meant a layer of a semiconductor material, having a crystallographic relaxation rate, as measured by X-ray diffraction or Raman spectroscopy, superior to 50%. A layer having a 100% relaxation rate, has a lattice parameter substantially identical to the nominal lattice parameter of the material of the layer, that is to say the lattice parameter of the material in its bulk form in equilibrium.

Conversely, the term "strained layer" means any layer of a semiconductor material whose crystallographic structure is strained in tension or in compression during crystal growth, such as epitaxy, requiring at least one lattice parameter to be substantially different from the nominal lattice parameter of this material.

Thus, a buffer layer makes it possible to grow an SiGe layer on an Si substrate without this SiGe layer being strained by the substrate.

Given that bulk SiGe is usually not available on the market, the use of a buffer layer in a wafer in order to have a relaxed SiGe layer on the surface thus makes it possible to produce a structure which can thus fulfil the same functions as a bulk SiGe substrate.

5 The buffer layer inserted between the Si wafer and the relaxed SiGe layer is generally made of SiGe, with a quantitywise proportion of germanium which progressively increases through the thickness of the wafer towards the relaxed layer.

Thus, it makes it possible to:

- 10 - gradually increase the germanium content from the wafer towards the relaxed layer;
- confine defects associated with the difference in lattice parameter so that they are buried;
- give a sufficiently thick relaxed SiGe layer stability with respect to
- 15 a film of different material grown epitaxially on its surface in order to strain the latter so as to modify its lattice parameter without influencing that of the relaxed SiGe layer.

For all these reasons, the buffer layer must be sufficiently thick, typically having a value greater than one micron.

20 Processes of transferring the layer of relaxed material grown epitaxially on such a buffer layer from the wafer on to a receiving substrate are known.

Such processes are, for example, proposed in an IBM document by L.J. Huang et al. ("*SiGe-On-Insulator prepared by wafer bonding and layer*
25 *transfer for high-performance field-effect transistors*", Applied Physics Letters, 26/02/2001, Vol. 78, No. 9) and in document WO 02/33746, in which documents an SGOI (Silicon-Germanium-On-Insulator) structure is produced from a wafer comprising in succession a single-crystal Si support substrate, an SiGe buffer layer and a relaxed SiGe layer.

30 One process employed in a document by L.J. Huang et al. consists in carrying out a Smart-Cut® process of the Applicant, known to those skilled in the art, and descriptions of which may be found in a number of works dealing with wafer reduction techniques, in order to remove the relaxed SiGe layer so as to transfer it by means of bonding on to an oxidized
35 receiving substrate, thus producing an SGOI structure.

Despite the advantages that this process affords, a few rough areas may form on the surface of the transferred layer and a surface finishing step then has to be carried out.

This finishing step is generally carried out by means of CMP

(chemical-mechanical polishing or chemical-mechanical planarization), which may create surface defects (such as strain-hardened regions), which may imperfectly correct the thickness, and thus retain inhomogeneous layer thicknesses, and which may slow down the transfer of the SiGe layer, and increase its cost.

The process presented in document WO 02/33746 includes, in addition to a CMP polishing step, preliminary lapping, polishing and etching steps in order to remove part of the wafer, thereby slowing down the overall process of removal from the wafer and increasing its cost even further, while not ensuring good homogeneity in layer thickness.

The abovementioned first object of the transfer is therefore not sufficiently achieved in this case.

To try to alleviate this, document US 5 882 987 and US 6 323 108 disclose an overall process for producing SOI (silicon-on-insulator) structures from a wafer comprising in succession a single-crystal Si support substrate, an SiGe layer and an epitaxially grown Si layer bonded to an oxidized receiving substrate.

The Smart-Cut® technique is employed and causes, after bonding the wafer to a receiving substrate, detachment of part of the wafer at the Si support substrate.

A structure consisting in succession of part of the Si support substrate, the SiGe layer and the epitaxially grown Si layer is thus removed, the whole assembly being bonded to the oxidized receiving substrate.

Two successive selective etching operations are then carried out on the structure in order to remove firstly the remaining part of the Si support substrate with an etching solution such that the SiGe layer forms a stop layer and then in order to remove the SiGe layer with an etching solution such that the Si layer forms a stop layer.

The structure obtained at the end is an SOI structure with a surface Si layer.

Thus, an SeOI structure is obtained with a semiconductor layer which is both thin and uniform through the thickness, substantially identical to the epitaxially grown initial layer, while avoiding the use of a finishing step other than a selective etching operation.

However, the SiGe layer inserted between the Si wafer and the epitaxially grown Si layer has a typical thickness of between 0.01 and 0.2 microns, a thickness which is insufficient, as mentioned above, to pretend to fulfil the role of a buffer layer between the Si wafer and a

potential relaxed SiGe layer.

The wafer therefore does not include a buffer layer.

The abovementioned second object of the transfer is therefore not achieved in this case.

5 In addition, given the order of magnitude of the thickness of the inserted SiGe layer, the structural (strained, relaxed or intermediate) state of the latter does not seem defined with certainty.

Now, another main objective of the transfer relates also to the production of a final structure comprising one or more layers in substantially controlled structural states, such as a substantially relaxed SiGe layer, something which does not seem to be guaranteed in the production of a structure described in the document US 6 323 108.

10 As regards document WO 01/99169, this provides processes for producing, from a wafer consisting in succession of an Si substrate, an SiGe buffer layer, a relaxed SiGe layer and optionally a strained Si or SiGe layer, a final structure with the relaxed SiGe layer on the optional other strained Si or SiGe layer.

15 The technique employed for producing such a structure involves, after bonding the wafer to a receiving substrate, removal of the material of the wafer that it is desired not to retain, by selectively etching the Si substrate and the SiGe buffer layer.

20 Although it transpires that this technique does make it possible to achieve particularly small layer thicknesses which are homogeneous through the thickness, it entails, however, destruction of the Si substrate and the SiGe buffer layer by chemical etching.

These processes therefore do not allow the possibility of reusing part of the wafer, and especially at least part of the buffer layer, for a further transfer of layers.

25 The third object of the transfer mentioned at the start of the document is therefore not achieved in this case.

WO 02/15244 document describes a source wafer, provided before transfer, comprising relaxed SiGe layer/strained Si/SiGe layer / buffer SiGe layer / Si substrate structure.

30 Then, the transfer consists doing a Smart-Cut® process at the strained Si layer level.

Implanting ions in the strained layer of Si can be difficult to operate due to the thickness of a such layer, and can thus lead to creation of structural damages inside the SiGe layers surrounding it.

In order in particular to achieve these objectives, the present

invention provides, according to a first aspect, a method of producing a structure comprising a thin layer of semiconductor material obtained from a wafer, the wafer comprising a lattice parameter matching layer comprising an upper layer of a material chosen from semiconductor materials having a first lattice parameter, characterized in that it comprises the following steps :

(a) growth of a film of a material chosen from semiconductor materials on the upper layer of the matching layer, which film being of material having a nominal lattice parameter substantially different from the first lattice parameter, wherein the grown film has a thickness small enough to keep the first lattice parameter of the upper layer of the underlyed matching layer and thus to be strained;

(b) growth of a relaxed layer of a material chosen from semiconductor materials on the film, the said layer having a nominal lattice parameter substantially identical to the first lattice parameter;

(c) removal of at part of the wafer, comprising the following operations:

- formation of an embrittlement zone in the matching layer; and
- supply of energy in order to detach, at the embrittlement zone level, the part of the wafer comprising the relaxed layer, thus forming the structure to produce.

Further characteristics of the method according to the invention are the following :

- after step (b), an additional step is carried out in which a receiving substrate is bonded to the wafer on the relaxed layer side;
- in this case, the receiving substrate is made of silicon;
- in either of these latter two cases, before bonding, a step of forming at least one bonding layer between the receiving substrate and the wafer is furthermore carried out, the bonding layer being formed on the receiving substrate and/or on the bonding face of the wafer;
- in the latter case, the bonding layer is an electrically insulating material such as silica;
- the embrittlement zone is formed by implantation of species into the matching layer at a depth substantially equal to the implant depth;
- before step (b), the embrittlement zone is formed by porosification of a layer beneath the relaxed layer;
- step (c) comprises, after the energy supply operation of step (c), at least one selective etching operation;
- in one of the latter two cases, a selective etching operation relates

to the etching of the remaining part of the matching layer with respect to the film (after detachment of the wafer by energy supply) ;

- it further comprises a growth of a semiconductor material on the film, the semiconductor material is substantially the same as the one of the film

5 (3) ;

- it further comprises an oxidation of the film;

- an annealing treatment is operated at the same time or following the oxidation, this annealing treatment being able to strengthen the bonding interface.

10 - in the latter case, a selective etching operation relates to the etching of the film with respect to the relaxed layer;

- the process furthermore comprises, after step (c), a step of growing a layer on the relaxed layer;

15 - in this case, the growth layer on the relaxed layer is made of strained material;

- the matching layer is made of silicon-germanium (the matching layer comprising a buffer layer with a germanium concentration which increases through the thickness and a relaxed layer beneath the film), the film of strained material is made of silicon, the relaxed layer is made of

20 substantially relaxed silicon-germanium (with a germanium concentration substantially equal to the germanium concentration of the relaxed layer of the matching layer);

- in the latter two cases, the growth layer produced on the relaxed layer is made of strained silicon so as to substantially preserve the lattice

25 parameter of the subjacent relaxed silicon-germanium layer;

- the wafer comprises at least one layer furthermore containing carbon with a carbon concentration in the layer substantially less than or equal to 50% ;

30 - the wafer comprises at least one layer furthermore containing carbon with a carbon concentration in the layer substantially less than or equal to 5%.

According to a second aspect, the invention provides an

- intermediate structure obtained during implantation step of a process according to the invention, comprising in succession a substrate, a

35 lattice parameter matching layer comprising an upper layer having a first lattice parameter, a film of strained material having a nominal lattice parameter substantially different from the first lattice parameter, and a layer made of substantially relaxed material having a nominal lattice parameter substantially identical to the first lattice parameter;

According to a third aspect, the invention provides an application :

- the productions of one of the following "semiconductor on insulator" structures : SGOI, strained Si / SGOI, SiGe / strained Si / SGOI, SiO₂ / SGOI;

5 - the structure "semiconductor on insulator" comprises a semiconductor layer containing carbon.

Further aspects, objects and advantages of the present invention will become more clearly apparent on reading the following detailed description of the implementation of preferred processes of the invention, these being
10 given by way of non-limiting example and with reference to the appended drawings in which:

Figure 1 shows the various steps of a method of producing an electronic structure comprising a thin SiGe layer according to the invention.

An example of a method according to the invention will now be
15 described below, which starts, with reference to Figure 1a, from a wafer 10 consisting in the first place of a single-crystal silicon support substrate 1 and an SiGe lattice parameter matching layer 2.

The expression "lattice parameter matching layer" denotes any structure behaving as a buffer layer and having, on the surface, a layer of
20 substantially relaxed material without an appreciable number of structural defects, such as dislocations.

Thus, in our example, it will be advantageous to choose an SiGe matching layer 2 consisting in succession of an SiGe buffer layer and a relaxed SiGe layer on the surface.

25 The buffer layer preferably has a germanium concentration which grows uniformly from the interface with the support substrate 1, for reasons which were explained above. Its thickness is typically between 1 and 3 micrometers in order to obtain good structural relaxation on the surface.

The relaxed SiGe layer has advantageously been formed by epitaxy
30 on the surface of the buffer layer and its thickness may vary widely depending on the case, with a typical thickness of between 0.5 and 1 micron.

The germanium concentration in the silicon within the relaxed SiGe layer is not limited in terms of value, but is preferably greater than 15% in
35 order to obtain, during the next step (shown by Figure 1b), a grown strained Si film 3, and is typically between 15% and 30%, but may be greater than 30%.

This 30% limitation represents a typical limitation in the current technique, but this may be caused to change in the coming years.

With reference to Figure 1b, an Si film 3 is grown on the SiGe matching layer 2.

In a first case, the film 3 is grown *in situ*, directly in continuation with the formation of the subjacent matching layer 2, the latter also being in this case advantageously formed by layer growth.

In the second case, the film 3 is grown after a gentle finishing step carried out on the surface of the subjacent matching layer 2, for example by CMP polishing.

The Si film 3 is advantageously formed by epitaxy using techniques such as CVD (chemical vapour deposition) and MBE (molecular beam epitaxy) techniques.

The silicon of the film 3 is then obliged by the matching layer 2 to increase its nominal lattice parameter in order to make it substantially identical to that of its growth substrate and thus introduce internal tensile strains.

It is necessary to form quite a thin Si film 3 - this is because too great a film thickness would cause the strain in the thickness of the film to relax towards the nominal lattice parameter of the silicon and/or defects to be generated in the film 3.

The thickness of the film 3 is thus typically less than 200 angstroms in order to avoid any relaxation of the strain therein.

Referring to Figure 1c, a relaxed SiGe layer 4 is grown on the strained Si film 3, advantageously by epitaxy (for example by CVD or MBE).

This relaxed SiGe layer is produced either *in situ*, immediately after growth of the subjacent film 3, or after a soft finishing step carried out on the surface of the subjacent film 3, such as a CMP polishing step.

The Ge concentration in this layer 4 is substantially the same as that present near the bonding face of the matching layer 2, so as to keep the nominal matching parameter of the relaxed SiGe layer present at this level in the matching layer 2 and preserved in the strained Si film 3.

The thickness of this relaxed SiGe layer 4 may be from a few tens to a few hundreds of nanometres, preferably between 10 and 100 nanometres.

With reference to Figure 1d, a receiving substrate 5 is advantageously bonded to the relaxed SiGe layer 4.

This receiving substrate 5 may, for example, be made of silicon or may consist of other types of materials.

The receiving substrate 5 is bonded by bringing it into intimate contact

with the relaxed layer 4, advantageously effecting molecular adhesion (wafer bonding) between the substrate 5 and the layer 4.

This bonding technique, as well as variants, is especially described in the document entitled "*Semiconductor Wafer Bonding*" (Science and
5 Technology, Interscience Technology) by Q.Y. Tong, U. Gösele and Wiley.

If necessary, bonding is accompanied by an appropriate prior treatment of the respective surfaces to be bonded and/or by supplying thermal energy and/or supplying an additional bonding layer.

Thus, for example, a heat treatment carried out during bonding allows
10 the bonds to be strengthened.

Bonding may also be reinforced by a bonding layer inserted between the layer 4 and the receiving substrate 5, which makes it possible to produce molecular bonds both with the layer 4 and with the material constituting the bonding face of the receiving substrate 5 which are at least
15 as strong as those existing between the layer 4 and the receiving substrate 5.

Thus, silicon oxide (also called silica or SiO_2) is a material that may be chosen for producing such a bonding layer. The silica may be formed on the relaxed layer 4 and/or on the receiving substrate 5, by SiO_2 deposition
20 or by thermal oxidation on the respective bonding surfaces.

Advantageously, the material constituting the bonding face of the receiving substrate 5 and/or the material of the bonding layer optionally formed is electrically insulating, in order in the end to produce an SeOI structure 20, the semiconductor layer of the SeOI structure then being the
25 transferred relaxed layer 4.

Once the receiving substrate 5 has been bonded, part of the wafer 10 is removed in order to transfer the relaxed SiGe layer 4 on the receiving substrate 5 and thus produce the desired structure 20.

Substantially all that part of the wafer 10 on the matching layer 2 side
30 in relation to the relaxed SiGe layer 4 is removed.

With reference to Figures 1e and 1f, this material removal is carried out in two steps:

A first step of material removal, shown in Figure 1e, consists in removing substantially the entire part of the wafer 10 on the matching layer
35 2 side in relation to the film 3.

To do this, a first material removal operation consists in detachment the donor wafer in a region of the matching layer 2 that has been weakened beforehand in this region.

Two known non-limiting techniques may thus carry out such an

operation:

A first technique, called the Smart-Cut® technique, known to those skilled in the art (and descriptions of which may be found in a number of works dealing with wafer reduction techniques), consists in implanting atom
5 species (such as hydrogen ions) and then in subjecting the implanted region, which then forms an embrittlement zone, to a heat treatment and/or mechanical treatment, or another supply of energy, in order to make the detachment in the embrittlement zone.

Detachment an embrittlement zone thus formed in the matching layer
10 2 makes it possible to remove most of the wafer 10, in order to obtain a structure comprising the remainder of the matching layer 2, the strained Si film 3, the relaxed SiGe layer 4, the optional bonding layer and the receiving substrate 5.

A second technique consists in obtaining a weak interface by creating
15 at least one porous layer, as described for example in document EP-A-0 849 788, and then in subjecting the weak layer to a mechanical treatment, or another supply of energy, in order to make the detachment in the weakened layer.

This weakened layer made of porous silicon is formed within the
20 support substrate 1, between the support substrate 1 and the matching layer 2, in the matching layer 2 (for example between a buffer layer and a relaxed layer) or on the matching layer 2 (that is to say between the matching layer 2 and the strained Si film 3).

To form a weakened layer within the support substrate 1, the porous
25 layer is advantageously formed on a single-crystal Si wafer and then a second growth is carried out on the porous layer, so as to grow a non-porous Si layer having substantially the same lattice parameter as the Si of the wafer; the support substrate 1 then consists of the wafer, the porous layer and the non-porous Si layer.

30 A detachment at the weakened layer makes it possible to remove at least some of the wafer 10, in order to obtain a structure comprising the optional remainder of the wafer 10, the strained Si film 3, the relaxed SiGe layer 4, optionally the inserted bonding layer and the receiving substrate 5.

A treatment of the wafer 10, in order to remove the porous silicon
35 which remains after the detachment, is advantageously carried out, such as an etching operation or a heat treatment.

If the porous layer lies within the support substrate 1, a lapping, chemical-mechanical polishing and/or selective chemical etching operations are then advantageously carried out in order to remove the

remaining part of the support substrate 1.

These two non-limiting techniques make it possible to rapidly remove, en bloc, a substantial part of the wafer 10.

They also allow the possibility of reusing the removed part of the wafer 10 in another process, such as for example a process according to the invention.

Thus, if the part removed is the support substrate 1, an operation to reform a matching layer 2, a film 3 and a relaxed layer 4 may be carried out as described above, after the surface of the support substrate 1 has been polished.

A second material removal operation after detaching the wafer 10 according, for example, to one of the above two techniques, consists in removing, if necessary, the remaining part of the matching layer 2.

This operation may be carried out by selective chemical etching so that the strained Si film 3 undergoes little or no etching, this forming an etching stop layer.

The remaining part of the matching layer 2 is in this case etched by wet etching using etch solutions having substantial selectivities with respect to the strained Si film 3, such as a solution comprising HF/H₂O₂/CH₃COOH (approximately 1/1000 selectivity) or HNA (hydrofluoric-nitric-acetic solution).

Dry etching operations may also be carried out in order to remove material, such as plasma etching, or by sputtering.

This chemical method has the main advantage of being quite rapid for thin layers to be removed and of avoiding the use of chemical-mechanical polishing finishing operations usually employed after detaching the wafer.

However, the chemical etching operation may advantageously be preceded, especially in the case of a thicker layer to be removed, by mechanical or chemical-mechanical abrasion by lapping and/or chemical-mechanical polishing CMP of the remaining part of the matching layer 2.

These techniques are proposed by way of an example in the present document, but they do not in any way constitute a limitation, the invention covering all types of techniques suitable for removing material from a wafer 10 in accordance with the process according to the invention.

A first application of the invention implies a preservation of the film 3, at least partially, in order to produce a strained Si/SGOI structure.

Optionally, a growth of Si is operating on the film 3 to thicken it.

The obtained strained layer after growth should stay below the critical thickness.

As the last step of etching the remaining part of the matching layer 2 may have damaged or thinned the film 3, an advantage of thickening the film 3, is to get back the initial thickness, or a more important thickness (still below the critical thickness).

5 This thick strained Si layer can then be used as an active layer (taking thus advantage of electrons high mobility that a such material exhibits).

Optionally, the strained Si of the film 3, thickened or not during the previous option, is at least oxidized.

10 A first interest of this oxidation step is to encapsulate the underlayer of SiGe, avoiding a Ge diffusion from it.

A second interest is found if an additional annealing step is implemented in order to strengthen the bond at the bonding interface.

Other advantages may be found, as for instance, an improvement of the film 3 quality.

15 Indeed the bounding annealing step is generally carried out within a range of temperature that can create some defaults in the structure, as for instance pinholes. As describe in WO99/52 145, presence of a SiO₂ layer on a semiconductor layer avoids most of problems during annealing.

20 Using the Si of film 3 as the material to oxidize is all the more judicious than Si is easier to oxidize than SiGe material.

A second application of the invention implies a removal of the film 3 by a chemical way, as shown in Figure 1f.

25 To do this, it is preferred to use selective etching employing an etch solution exhibiting high selectivity with respect to the relaxed SiGe layer 4, such as a solution comprising at least one of the following compounds: KOH (potassium hydroxide), NH₄OH (ammonium hydroxide), TMAH (tetramethylammonium hydroxide), EDP (ethylenediamine / pyrocatechol / pyrazine) or HNO₃, or solutions currently under study combining agents such as HNO₃, HNO₂H₂O₂, HF, H₂SO₄, H₂SO₂, CH₃COOH, H₂O₂ and H₂O, 30 as explained in document WO 99/53539, page 9.

This second step makes it possible to retain good surface quality and good thickness homogeneity of the relaxed SiGe layer 4.

Thus, a layer quality substantially identical to that obtained during its growth (shown in Figure 1c) is retained.

35 This is because this transferred layer 4 has not necessarily been subjected to external mechanical stresses, such as those generated by a CMP finishing step, thus avoiding the appearance of defects associated with such stresses.

However, in certain particular cases, soft polishing is carried out in

order to remove any slight surface roughness.

Thus, a final relaxed SiGe-on-substrate structure is obtained, and in particular a relaxed SiGe-on-insulator structure (also called an SGOI structure) if the subjacent material of the relaxed SiGe layer 4 is an electrical insulator.

In one particular application of this structure, any epitaxy may be carried out on the relaxed SiGe layer, such as epitaxy of another SiGe layer or epitaxy of a strained Si layer.

In the latter case, an Si/SGOI final structure would be obtained, the Si layer being strained.

Having completed the final structure, a finishing step may optionally be carried out, such as finishing treatments like, for example, a heat treatment in order to further strengthen the bonding interface with the receiving substrate 5.

The present invention is not limited to an SiGe lattice parameter matching layer 2, but also extends to a constitution of the matching layer 2 from other types of type III-V materials or other materials capable of straining the material of the epitaxially overgrown film 3.

The present invention is not limited to a film 3 of strained Si, but also extends to a constitution of it from other types of III-V materials or other materials capable to be strained by the underlying matching layer 2.

Finally, the present invention does not relate only to transferring a relaxed SiGe layer 4, but in general relates to transferring a layer of any type of semiconductor able to be transferred according to a process of the invention.

In the semiconductor layers, other constituents may be added thereto, such as carbon with a carbon concentration in the layer in question substantially less than or equal to 50% or more particularly with a concentration of less than or equal to 5%.

CLAIMS

1. Method of producing a structure comprising a thin layer of semiconductor material obtained from a wafer (10), the wafer (10) comprising a lattice parameter matching layer (2) comprising an upper layer of a material chosen from semiconductor materials having a first lattice parameter, characterized in that it comprises the following steps :

(a) growth on the upper layer of the matching layer (2) of a film (3) of a material chosen from semiconductor materials, said film (3) being of material having a nominal lattice parameter substantially different from the first lattice parameter, said grown film (3) having a thickness small enough to keep the first lattice parameter of the upper layer of the underlyed matching layer (2) and thus to be strained;

(b) growth of a relaxed layer (4) on the film (3), said relaxed layer (4) being of a material chosen from semiconductor materials having a nominal lattice parameter substantially identical to the first lattice parameter;

(c) removal of at part of the wafer (10) , comprising the following operations:

- formation of an embrittlement zone in the matching layer (2) ;
and

- supply of energy in order to detach, at the embrittlement zone level, the part of the wafer (10) comprising the relaxed layer (4), thus forming the structure to produce.

2. Method of producing a structure according to the preceding claim, characterized in that, after step (b), an additional step is carried out in which a receiving substrate (5) is bonded to the wafer (10) on the relaxed layer (4) side.

3. Method of producing a structure according to the preceding claim, characterized in that the receiving substrate (5) is made of silicon.

4. Method of producing a structure according to either of the preceding two claims, characterized in that, before bonding, a step of forming at least one bonding layer between the receiving substrate and the wafer (10) is furthermore carried out, the bonding layer being formed on the receiving substrate (5) and/or on the bonding face of the wafer (10).

5. Method of producing a structure according to the preceding claim, characterized in that the bonding layer is an electrically insulating material.

5 6. Method of producing a structure according to the preceding claim, characterized in that the bonding layer is made of silica.

7. Method of producing a structure according to the preceding claim, characterized in that the bonding layer is formed by thermal oxidation.

10

8. Method of producing a structure according to one of the preceding claims, characterized in that the embrittlement zone is formed by implantation of species into the matching layer (2) at a depth substantially equal to the implant depth.

15

9. Method of producing a structure according to one of claims 1 to 7, characterized in that, before step (b), the embrittlement zone is formed by porosification of a layer beneath the relaxed layer (4).

20

10. Method of producing a structure according to one of the preceding claims, characterized in that step (c) comprises, after the energy supply operation of step (c), at least one selective etching operation.

11. Method of producing a structure according to the preceding claim, characterized in that a selective etching operation relates to the etching of the remaining part of the matching layer (2) with respect to the film (3) (after detachment of the wafer (10) by energy supply).

12. Method of producing a structure according to the preceding claim, characterized in that it further comprises a growth of a semiconductor material on the film (3), the semiconductor film being substantially the same as the one of the film (3).

13. Method of producing a structure according to any of the two preceding claims, characterized in that it further comprises an oxidation of the film (3).

14. Method of producing a structure according to the preceding claim, characterized in that an annealing treatment is operated at the same time or following the oxidation, this annealing treatment being able to strengthen the bonding interface.

15. Method of producing a structure according to the claim 10 or 11, characterized in that a selective etching operation relates to the etching of the film (3) with respect to the relaxed layer (4).

10

16. Method of producing a structure according to one of the preceding claims, characterized in that it furthermore comprises, after step (c), a step of growing a layer on the relaxed layer (4).

17. Method of producing a structure according to the preceding claim, characterized in that the growth layer on the relaxed layer (4) is made of strained material.

18. Method of producing a structure according to one of the preceding claims, characterized in that:

- the matching layer (2) is made of silicon-germanium, the matching layer (2) comprising a buffer layer with a germanium concentration which increases through the thickness and a relaxed layer beneath the film (3);
- the film (3) of strained material is made of silicon;
- the relaxed layer (4) is made of substantially relaxed silicon-germanium, with a germanium concentration substantially equal to the germanium concentration of the relaxed layer of the matching layer (2).

19. Method of producing a structure according to the two preceding claims, characterized in that the growth layer produced on the relaxed layer (4) is made of strained silicon so as to substantially preserve the lattice parameter of the subjacent relaxed layer (4).

20. Method of producing a structure according to one of the preceding claims, characterized in that the wafer (10) comprises at least one layer furthermore containing carbon with a carbon concentration in the layer substantially less than or equal to 50%.

21. Method of producing a structure according to one of the preceding claims, characterized in that the wafer (10) comprises at least one layer furthermore containing carbon with a carbon concentration in the
5 layer substantially less than or equal to 5%.

22. Intermediate structure obtained just after the implementation of the step (c) of the method according to one of claims 2 to 21, comprising in succession a substrate (5), a first layer having a first lattice parameter, a
10 film (3) of strained material, and an upper layer made of substantially relaxed material having a nominal lattice parameter substantially identical to the first lattice parameter, characterized in that the free surface of the upper layer exhibits features of post-detachment embrittlement zone surface.

15

23. Application of the method according to claims 1 to 20, to the productions of one of the following "semiconductor on insulator" structures :
SGOI ; strained Si / SGOI, SiGe / strained Si / SGOI ; SiO₂ / SGOI.

20

24 Application according to the preceding claim, characterized in that the structure "semiconductor on insulator" comprises a semiconductor layer containing carbon.

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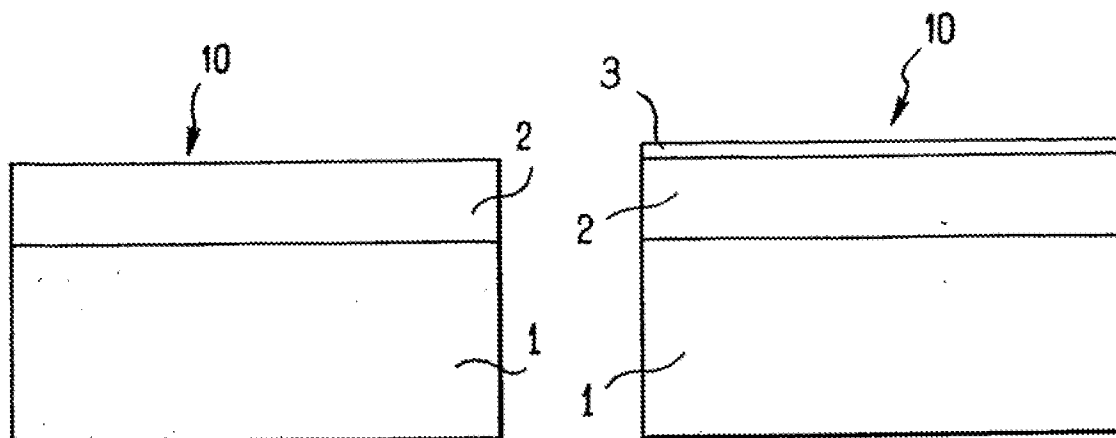


FIG. 1a

FIG. 1b

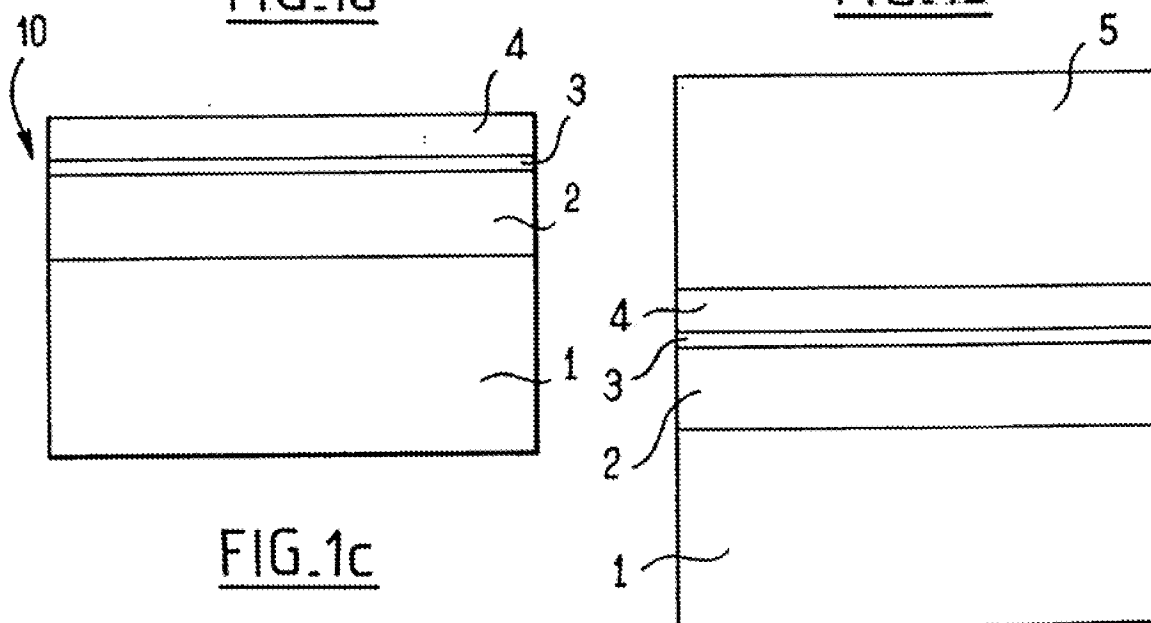


FIG. 1c

FIG. 1d

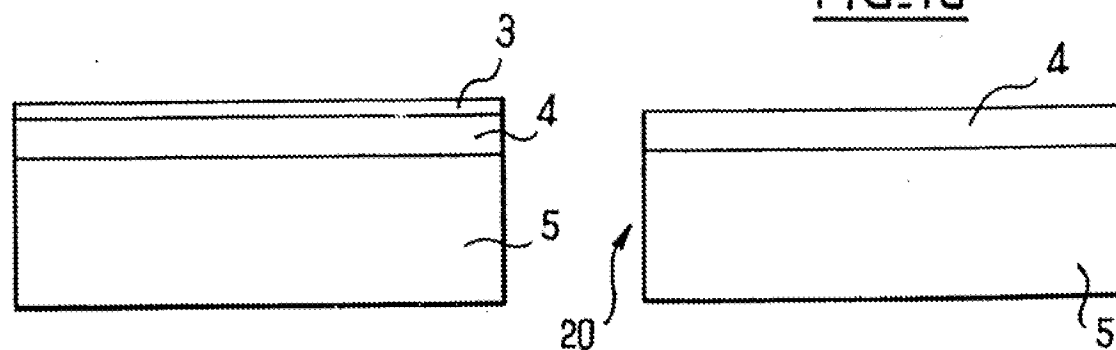


FIG. 1e

FIG. 1f